FINAL REPORT

on

ENGINEERING MODEL OF ANTENNA CAPACITANCE PROBE

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Contract No. NAS 5-9175

Prepared for:

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

Washington Technological Associates, Inc.
979 Rollins Avenue
Rockville, Maryland

Report No. NAS 9175-1

Approved by:

Project Engineer
WTA

Chief, Electronic Engineer
WTA

Project Scientist
NASA/GSFC

March 1966

ABSTRACT

This report describes the development of the Engineering Model of the Antenna Capacitance Probe, part number 2158-R-434, which is the prototype of an instrument to be carried aboard the Radio Astronomy Explorer (RAE) Satellite in a forthcoming mission. The instrument is designed to measure the effective capacitance of the RAE antenna in two frequency ranges (750 kc and 1mc). Thus the capacitance not only can be determined directly, but also a function of frequency. The output to telemetry is binary digits rather than analog signals, hence the frequency as a function of capacitance has a high degree of accuracy.

The expected radiation dosage influenced the selection of the semiconductors and the circuit design was based on h_{FE} derating to insure operation should higher dosage be encountered. If further longevity is desired, certain transistor substitution is suggested based on subsequent information and investigation.

An overall system operation is followed by a detailed operation of the individual circuit explanation, including the appropriate waveforms.

A detailed reliability and failure analysis shows that the probability of complete success is .956 and the probability of complete failure is .044.

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I. INTRODUCTION

This report describes the Engineering Model of the Capacitance Probe produced under Contract NAS 5-3759. This Capacitance Probe, is the prototype of an insturment to be carried aboard the Radio Astronomy Explorer (RAE) Satellite in a forthcoming mission. The purpose of the probe is to measure the capacitance which occurs between each of two antenna booms connected as dipoles, and the spacecraft skin. The antenna capacitance will be measured at two frequencies widely separated from each other. The instrument is designed as the RAE Antenna Capacitance Probe part number 2158-R-434.

The basic principle of measurement of the Capacitance Probe consists in reflecting the capacitance which exists between the two antenna booms, and the spacecraft skin to an oscillator which will change its operating frequency in direct proportion to the capacitance seen by the antennas. Each antenna boom is fed by a coaxial cable, and in order for these booms to look like a dipole antenna which is balanced to ground from each boom, some sort of impedance matching device is necessary. For this reason balun transformers are used in the oscillator circuit, the secondary of which acts as part of the tuned circuit of the oscillator. Since capacitance is a function of frequency, two oscillators are used, so that capacitance as a function of frequency can also be determined.

A plot of capacitance versus oscillator frequency is provided for each oscillator. Prior to launch the capacitance of the antenna base, coaxial cable,

and the oscillator capacitance can be determined. Thus by subtracting out this total predetermined capacitance from the capacitance as measured by the oscillator the antenna capacitance can be determined.

Each oscillator is completely enclosed in a metal container which is temperature monitored. In addition, a calibrating capacitor is provided so that oscillator drift can be detected if it occurs and the readings compensated for. The overall system then produces frequencies which are directly related to the low frequency calibrate capacitance, high frequency capacitance, the antenna low frequency, and the antenna high frequency. These frequencies are then telemetered to ground so that a record is obtained of the antenna capacitance during flight.

The power to the Capacitance Probe will be turned off and on during the flight. This will reduce the power consumption and eliminate interference problems between other experiments.

II. SYSTEM OPERATION

The general principle of operation of the Antenna Capacitance Probe has already been outlined in Section I above. This will now be extended by a more detailed functional description of the instrument, which will be followed by a discussion of the theory of operation of the system. Detailed description of some of the circuits will be presented in section IV.

2.1 GENERAL SYSTEM OPERATION

A block diagram of the Antenna Capacitance Probe is shown in Figure 1. The experiment is run synchronously from the 400 cps spacecraft clock. Upon receiving the power to the experiment, a minimum of 2.5 seconds is required for oscillator stability. At some time thereafter the programmer can initiate the accumulate or read command, which arrives as a pulse shifting from +6 volts (off) to 0 volts (on). The Capacitance probe, upon receipt of this command clears the counter, shift register and control circuitry by using this accumulate pulse as a reset.

Once the experiment is reset the oscillator frequencies are gated to the counter. The sequence of the frequencies going to the counter are: low frequency calibrate; 750 kcs; high frequency calibrate, 1 mcps; antenna low frequency; antenna high frequency. This sequence is internally controlled from the control logic circuitry by use of OR and NAND gates. The output of the oscillators are shaped for counter triggering by the squaring circuitry.

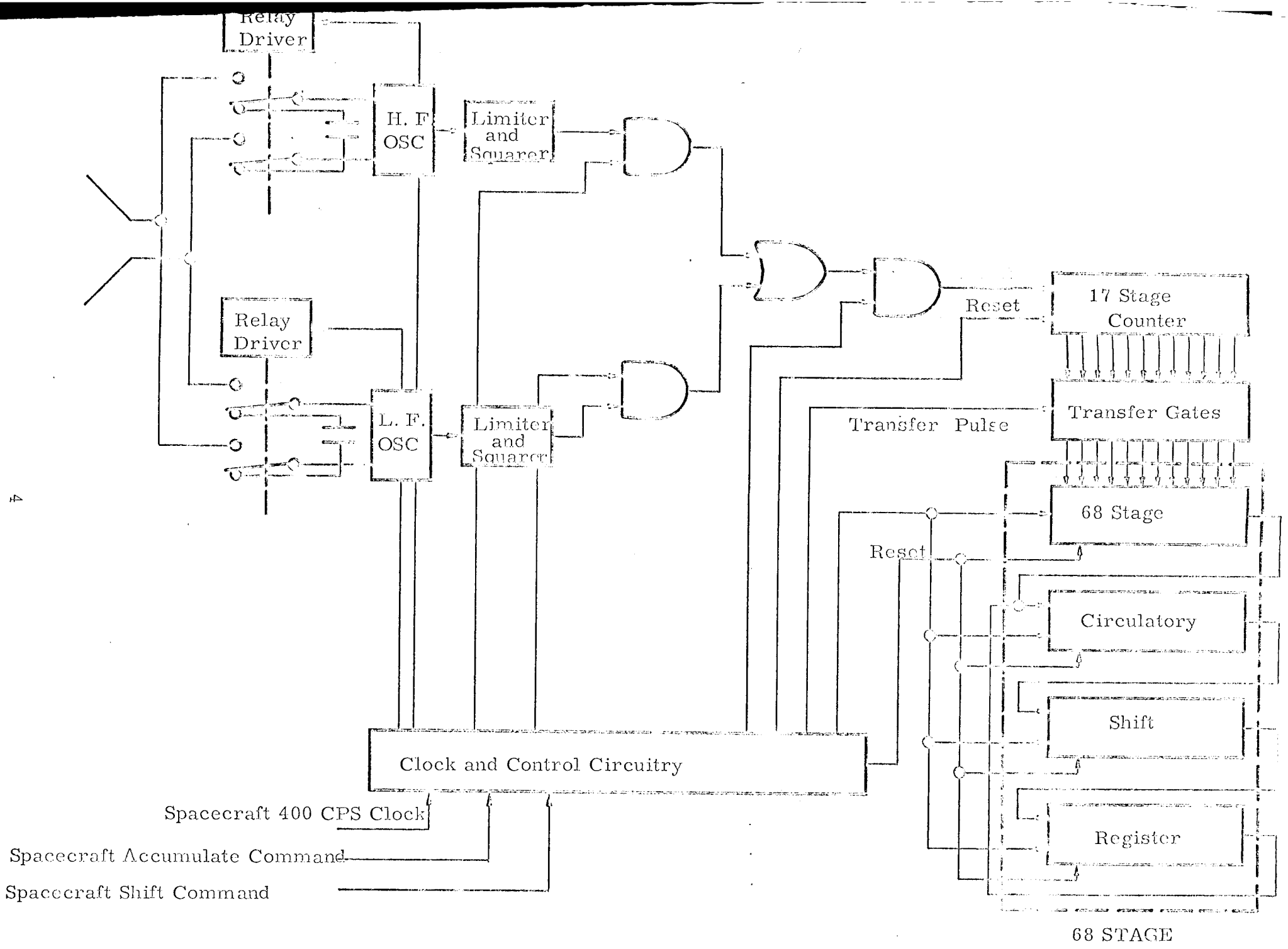

Figure 1. 1-Block Diagram Antenna Capacitance Probe

After each input to the counter which lasts exactly for 100 milliseconds, the counter input is temporarily disabled while the parallel transfer of information from the counter to the shift register is made and the counter is reset. The counter then accepts the next frequency. During this count time the information in the shift register is serially shifted down 17 stages to make room for the following parallel transfer to the shift register.

After four inputs to the counter, which requires 480 milliseconds, the shift register is full and the control circuitry will allow it to accept no more information, by disabling the transfer and shift pulse lines.

The information now contained in the shift register in binary digits is ready to be sent to telemetry upon receipt of the Shift Command. Some convenient period of time after the 480 milliseconds required to fill the register, the shift command will occur in the form of a gating pulse to a NAND gate, shifting from a off-state potential of +6 V to a on potential of zero volts and lasting for at least some integal multiple of 168.75 milliseconds. This is to allow 68 pulses from the 400 cps spacecraft clock pulse, which is the other input of the NAND gate, to shift the information from the register out to telemetry. Since this is a non-distruct circulatory type of shift register, at the end of the 68th pulse the information will have been completely shifted out, but also will be repositioned in the register identically to its position before the arrival of the shift command.

The information to telemetry is in the form of binary digits rather than analog signals, thus enabling each bit of frequency to be read. However some bit may be dropped or lost due to noise in transmission and for this reason it may be desirable to shift the information out twice, since no parity code has been provided.

Upon the completion of the shift pulse, when all the information stored in the register has been sent to telemetry the programmer may shut off the power to the Capacitance Probe, and the antennas can now be time shared with another experiment.

III. RADIATION EFFECTS ANALYSIS

3.1 INTRODUCTION

The requirement for radiation hardening is due to the fact that the RAE Satellite is to be flown in an orbit lying in the Van Allen belt. This is a circular orbit at an altitude of 6000 km inclined 50° to the equator. Because the intended service life of the satellite is at least one year, this means that the instruments will be in a radiation environmnet for 10,000 hours or more. Electronic components, such as resistors, capacitors, coils and insulators having been tested repeatedly in various radiation environments, have shown that they are orders of magnitudes less sensitive to radiation than most semiconductors. Therefore, it is reasonable to conclude that the maximum radiation tolerant level, that is the threshold failure, will be primarily determined by the semiconductors, In addition, the circuit design based on reduced gain will have a direct bearing on circuit failure due to radiation dosage. Since semiconductor devices are the most sensitive components to space radiation, this anaylsis is limited to the semiconductor devices of the Capacitor Probe.

3.2 TYPE OF NUCLEAR RADIATION EXPECTED

A combination of nuclear radiation environment may be encountered by a space vehicle passing through the Van Allen belts. Some of the types of radiation are, the steady state trapped radiation, cosmic radiation, auroral radiation and solor flare radiation. The greatest electronic failure damage to space electronic system in earth orbit is due to trapped particles which are the Van Allen electrons

and protons plus the Starfish explosion. Although the Starfish electron levels at the higher altitudes have not decayed as quickly, the electron levels in the lower portion of the electron belt have decayed by approximately an order of magnitude.

Cosmic radiation consist mainly of hydrogen nuclear (protons) having very high speed and whose energy is in the range of 1×10^{9} to 1×10^{10} electron volts. It is impractical to shield against cosmic particles of such great penetration.

Since the cosmic-particle flux is roughly about two particles per square centimeter per second. The ionization dose rate which can be attributed to cosmic radiation is in the vicinity of 10^{-4} rads per hour and that attributable to secondarily produced particles is about 10^{-3} rads per hour. Most materials and electronic components are uneffected until an ionization dose of 10^{-4} rads has been absorbed. Consequently cosmic radiation does not pose a severe threat to the performance of electronic equipment, especially when the materials and packaging are such as to reduce the secondary radiation or ionization effects. That is, complete potting of package to reduce any air space, and the restriction of materials such as teflon, Kel-F and the like. Although certain amounts of radiation effects can be annealed out by subjecting the electronic components to high temperatures, the temperature environment of the spacecraft is for too low for any efficient annealing to take place.

The innear Van Allen belt beginning somewhere between 399 to 1199 kilometers depending upon the latitude, and extending from about 45° north magnetic latitude

to 45° south magnetic latitude is made up mainly of a large number of electrons and protons of various kinetic energies all trapped by the earth's magnetic field.

Since radiation energy may be supplied in two forms: electromagnetic radiation, such as X- and gamma rays; or as particle radiation. The particles comprising the second basic form of radiation energy can be positively charged protons, negatively charged electrons or uncharged neutrons which are moving at speeds slower than that of light.

For charged particles, the interaction between the particle and an atom of the struck material produces a displacement which is caused by the electrostatic force between the nuclear charge and the moving particle. This displacement will occur if the charge particle has sufficient energy and if it passes within the radius of the inner most electron orbit. Uncharged particles such as neutrons, however, must pass within the much smaller radius of the atomic nucleus. If electrons have sufficent kinetic energy that is energies greater than 200 kev, they will create displacement. Since electrons of energies greater than 200 kev comprise less than 10% of the total in the Van Allen belts, displacements by electrons are not a major concern. However, whether the electrons originate in the Van Allen belt or as secondary electrons produced by gamma radiation they create the same effect.

Secondary electrons produced by gamma radiation processes can attain energies in excess of 200 kev. For primary electrons with energies ranging from 40 to 50 million electron volts, the energy is expended in the form of braking radiation, which is a complete conversion from the electron into gamma radiation. The threat from electrons in space radiation environment is due more from

contributions to the total ionization dose than from displacement damages. Although the average energy of electrons in the belt allows shielding, the secondary radiations they create is more troublesome. Protons are the most penetrating type of charged particle radiation in the Van Allen belts because of their higher average energy and their larger mass. Shielding against protons, therefore is difficult.

3.3 RADIATION ESTIMATES

Due to the spacecrafts orbit it has been estimated that the radiation dosage will be: 2.2×10^{12} electrons per cm^2 per year having kinetic energies greater than .5 mev; and 10^4 protons per cm^2 per second having kinetic energies greater than 30 mev. Further, it has been estimated that the spacecraft will provide a shielding density of .63 grams per cm^2 and the package will provide a shielding of .4 grams per cm^2. If it is assumed that this shielding will be done with aluminum then all the constant troublesome radiation effects will be due totally to protons having kinetic energies greater than 20 mev, as the shielding will be sufficient to effectively shield against all but the most energetic electrons (3 mev)[3].

Definite conclusions and expectations concerning nuclear radiation damage are not possible at this time, due partly to insufficient investigations, results and methods which are not totally compatible. Although it is well known that the radiation resistance of semiconductors can vary between batch lots of the same type for any given manufacturer it has also been generally agreed that some methods

of manufacturers are better than others for reducing failure due to nuclear radiation. Germaniun it would seem is better in general than sicilon, however, trade-offs exist when the circuit use is considered.

Although the transistors selected for use in the Capacitance Probe do not necessarily represent ones having the highest possible radiation resistant characteristics; they were chosen consistent with the current available information as to preferred type, previous performance, and radiation testing results. They

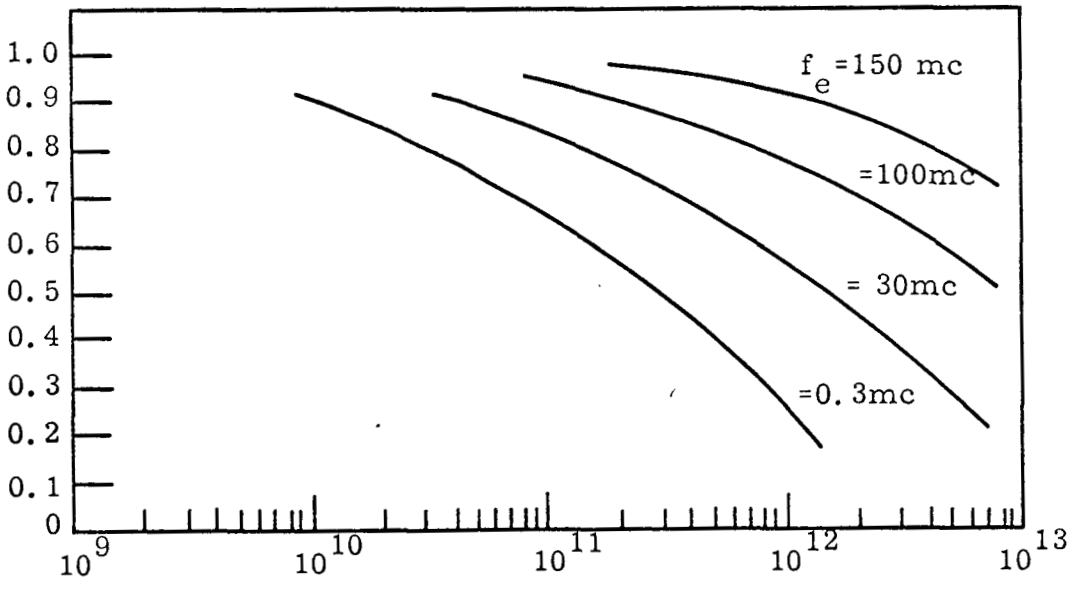

Figure 3.1-NEUTRON EXPOSURE (NVT, E >.1MEV)

are of the high f_T and low breakdown voltage type. The low breakdown voltage is also a requirement in the design of other radiation tolerant semiconductor devices, namely diodes. Semiconductor radiation dosage in laboratory testing have, because of convience, been exposed mainly to neutrons rather than electrons or protons, therfore in order to reduce all data to common terms, the proton and electron rates can be reduced to equivalent neutron dose rates. For protons the average figure which can be used for a close equivalence is to multiply the proton

rate by 4.2; for electrons, multiply the rate by 0.01 in order to get the equivalent neutron rate.

The susceptibility of transistors to radiation is a function of the transit time across the base region and, thus is a function of the transistor alpha cut-off frequency.[5] Degradation in transistor alpha as a function of neutron flux for various alpha cutoff transistors is shown in Figure 3.1. By converting the expected dosage of electrons and protons to equivalent total dosage of neutrons, the expected dosage would be 11.2×10^4 neutrons per square cm per second.

The alpha cutoff frequency of the 2N930 is 30 Mc. From Figure 3.1 a total dose of 41×10^{11} n/cm^2 would be required for the alpha to decrease to a value 0.7 of its initial value, which means that if no derating is done in the circuit design, the 2N930 could remain in orbit 1.16 years before its alpha degrades to 0.7 of its initial value. Actually in every discrete circuit of the Capacitance Probe the circuits have been designed to work with the common emitter gain lower than 0.5. The alpha cutoff frequency of the 2N2604 and 2N915 are 100 Mc and 400 Mc respectively and therefore have greater lifetimes than the 2N930.

An effective increase in the lifetime can be obtained by the substitution of 2N918 transistor for the 2N929 and 2N930, and substituting 2N3251 for the 2N871. This would mean that the lowest alpha would be 200 Mc; that is, the life would be extended to better than 8.3 years before the lowest alpha cutoff transistor would be degraded to 0.7 of its original value.

Similarily, the selection of the inegrated circuits used in the Capacitance Probe are those whose past performance in space and radiation test results indicate that they would survive the expected exposure in the Van Allen belt. There have not been many studies performed in integrated circuits since they are relatively new. However, those which have been performed conclude that the integrated circuits will be as radiation resistant as the same circuit makeup with compatible discrete components. Those Texas Instrument (series 51) circuits which were tested[6] showed that first failures occured at about 1.8×10^{14} n/cm^2 which is an order of magnitude above that discussed above. One possible means of improving the radiation resistance of these units, which could easily be incorporated in later units if deemed necessary, would be to decrease fan-out loading, since it has been found that there ia a direct correlation between fan-out and failure dosage.[4]

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IV. CIRCUIT DESCRIPTION

The individual part of the RAE Antenna Capacitance Probe will be discussed in some detail in this section of the report. The progression to be followed is:

4.1) Counter, transfer gates and shift register

4.2) Purpose of control logic

4.3) Functional operation of control gates

4.4) Control gates input and output timing signals

- 4.4.1 Oscillator gating
- 4.4.2 Transfer pulse
- 4.4.3 Relay Driver pulse
- 4.4.4 Reset pulse
- 4.4.5 Shift pulse

4.5) Development of control signals

4.6) Relay Driver circuitry

4.7) Oscillator circuitry

4.8) Limiting and squaring circuitry

4.9) Output buffer and send shifter

4.1 COUNTER, TRANSFER GATES AND SHIFT REGISTER

The frequency counting and storage circuitry, comprising the counter parallel transfer gates and circulatory shift register is shown in the overall schematic. The counter is made up of 17 conventional ripple through divide by two- binary frequency divider stages; stage 17 of which registers the most

significent bit. In using 17 binary stages to count 2 megacycle by accurately counting for 100 milliseconds the counter has the capability of counting a decimal number as high as 131,071. Since the counting time is .1 second or 100 milliseconds the conversion factor between the actual frequency of the oscillator and the number in the counter is 10, therefore the highest frequency capability of the counter is 1,310 710 cps. Although the calibaration frequency of the high frequency oscillator is one megacycle or 100,000 as read by the counter, it is not anticipated that the capability of the counter will be exceeded when the antenna is substituted for the calibrating capacitor. If however this should occur, the counter would begin counting over at a frequency of 131,172; hence the maximum frequency would be added to the frequency read out of the counter.

The last 15 stages of the counter are Texas Instrument SN5112 integrated circuit Flip-Flops, which are rated at a maximum of one megacycle. To insure the reliability of this counter, two high speed flip-flop, Signetics SE124G's were used for the first 2 stages, whereby the SN5112 will now see a maximum of 250 kcs. By using different I. C. components for the first two stages of the counter however, required that the logic levels be compatible, hence the inverter between the 2nd and 3rd stages. This compatibility requirement also caused an additional circuitry to be added to the reset line driving only the signetic stages. While all 17 stages of the counter reset from the same reset pulse, the last 15 T. I. stages only require one inverter, however, the first two high frequency Signetic stages require 2 inverters in the reset line for logic compatibility.

The transfer gates are Texas Instrument SN516A operated as Nand Gates. If the side of the counter stage driving a transfer gate is a "one" when the transfer pulse occurs, then this "one" is transferred to the appropriate shift register. The transfer of information from the counter to the shift register is done in parallel with the occurance of the transfer pulse, however serial transfer is performed once the information is in the register with the occurance of shift pulses.

The first 17 stages of the shift register areT. I.'s SN5111, the 51 following are SN510's, the reason for the difference being that the first 17 stages accept the information from the counter, therefore must have the capability of set, reset, and shift pulse, while the 51 following stages only need the capabilities of reset and shift pulse.

The register being a uni-directional circulating type of shift register necessitates that the output of the 68th stage be connected to the first stage which is shown in the overall schematic diagram. Thus shifting one bit at a time, requires 68 shift pulses for all information to be fed to telemetry. This shift rate occurs at a 400 cps rate which would thus require 170 milliseconds for the total transfer of information to be shifted out, and the information to be placed in its initial position within the register.

All stages of the register are essentially of the RS type and the interconnections between stages are indentical. Since a shift register requires temporary storage between two adjacent flip-flops. The state of one flip-

flop being changed is stored and used as the input to the subsequent flip-flop stage. That is the steering diodes or circuitry of the nth stage are tied to the nth-1 stage and the output of the nth stage drives the nth+1 stages steering circuitry.

4.2 CONTROL LOGIC

The purpose of the control logic circuitry is to generate timing pulses at the correct time and of the correct length which will:

(a) control which oscillator is on

(b) control the mode of the oscillator (antenna or calibrate)

(c) control the length of time an oscillator is on

(d) shift the register

(e) transfer the information in the counter to the register

(f) reset the counter

(g) control the counting time of the counter

(h) prevent the register from over flowing before shift out command

(i) provide shift out upon shift command

The only input to the control logic circuitry are the 400 cps clock pulse, the read or accumulate command and the shift command. Hence the proper control pulses are generated internally using these three input signals and Texas Instrument and Signetics integated circuits; specifically Flip-Flops, Nand Gates, OR Gates, oneshot multivibrators and "clock" drivers.

4.3 FUNCTIONAL OPERATION OF CONTROL GATES

In the interest simplicity and clarity a step-by-step operational description will be presented, followed by the timing signals generated internally and applied to the control gates and interface circuitry between the gates and counter-memory circuitry. Subsequently the generation of the timing signals will be discussed.

Assume that the information contained in the register has been sent to telemetry and that the power has been shut-off, then at some time t_n, the power is reapplied. A minimum delay of 2.5 seconds (tn+ 2.5 sec.) is required for oscillator stability before the Read Command can be applied; hence the read command occurs at tn + 2.5 + t acting as a reset pulse. The reset or Read command pulse resets the counter, logic circuitry and clears the shift register.

Immediately after the reset, the low frequency oscillator in the calibrate mode is allowed through the NAND gate A HG1/2 (terminal 2 of gate A HG1) and through the OR gate A HG1/2, 9, 10 (terminals 2, 9 and 10 connected together form one output); the low frequency calibrate is prevented from reaching the counter for 20 milliseconds however, by Nand gate A HG2/9, 2.

During this 20 millisecond delay the following things occur: (2) 5 milliseconds after the reset or read command, the transfer pulse is applied to the transfer gates, (b) 10 milliseconds after reset, the counter is reset.

At the completion of the 20 millisecond delay the Nand gate A HG2/92 is opened for exactly 100 milliseconds and the low frequency calibrate signal is allowed to pass to the counter. During this 100 milliseconds interval while the counter accepts and counts the low frequency calibrate signal, there are 17 shift pulses applied to the shift register, at a rate of 200 cps. The shift pulses occur 27.5 milliseconds after the counter begins counting and since it takes 82.5 milliseconds for the 17 pulses to be applied, the shift pulses last until the counter is gated off.

At the same instant the counter is gated off the low frequency calibrate signal is gated off and the high frequency calibrate oscillator signal is allowed to pass through the Nand gate A HG1/10 and the OR gate A HG1/9, 2.10 but is delayed in passing to the counter again for 20 milliseconds while the transfer pulse and counter reset pulse is applied as previously explained. At the end of the 20 millisecond delay the Nand gate A HG1/92 is again opened for exactly 100 milliseconds and the counter accepts this frequency. Again while this is happening the information now contained in the first 17 stages of the shift register (low frequency calibrate) is shifted to the second 17 stages of the shift register by the 17 shift pulses passing through the Nand Gate C-G3/8, and OR gate C-G3/8, as previously explained.

At the completion of the second 100 millisecond count the high frequency calibrate is prevented from reaching the counter by the Nand gates, and the following things occur: the Nand gate B-G7/8 applies a positive pulse which

energizes the relay driver for the low frequency oscillator; the Low frequency Nand gate A HG1/2 is opened. Thus the frequency as seen from the antenna capacitance is fed to the Nand gate A HG2/92. Again this gate is prevented from opening for the 20 millisecond period while the high frequency calibrate signal, still contained in the counter, is dumped into the first 17 shift register stages with the transfer pulse which occurs 5 milliseconds after the start of the 20 millisceond delay, and the counter is reset again at 10 milliseconds in this 20 millisecond period. Following this 20 millisecond delay the counter accepts the antenna determining low frequency signal while the previous 2 signals are shifted down the register 17 stages.

Upon completion of the 3rd count the signal from the low frequency oscillator is disabled from reaching the counter and the low frequency relay driver is disabled.

However, at the instant the low frequency relay driver is de-energized, the high frequency relay driver is energized by a positive pulse from the output of Nand gate B-G6/8 and the read and shift cycle is completed identically to that of the low frequency cycle above. Thus at the completion of the 4th 100 millisecond count period there is information in the counter and in shift register stage 18 through 68.

If there was nothing to shut off this total read-in cycle the whole procedure would repeat at this point- in fact it starts too. However, during the 5th 20 millisecond delay period, not only is the information in the counter put in the

first 17 stages of the shift register, filling it, and the counter cleared, but at the completion of the 20 millisecond delay,the state of flip flop B-FF14 changes so that the Nand gate B-G7/4 will pulse flip flop C-G2/8 and B-G4/9 is disabled until another read command occurs reseting B-FF11. While the counter will continue to count there will be no further transfer pulses occuring to dump the counter information into the shift register; the only shift pulses which can now occur are generated by the shift command which would apply 68 pulses from the spacecraft 400 cps clock through Nand gate C-G3/4 and OR gate C-G3/8 to shift the information contained in the shift register to telemetry at the same time re -circulating the information within the register.

4.4 CONTROL GATES INPUT AND OUTPUT TIMING SIGNALS

The inputs and outputs to the above gates and the counter memory interface circuitry will be shown consistant with the assumptions made previously. It is important to note at the outset that all T. I. 's Nand gates use logic levels which are complimentary to those of the Signetic Nand gates; failure to do so will result in improper synchronization of the relay drivers.

4.4.1 Oscillator Gating

As shown in Figure 4. 1A, the gating signal to the Nand gates controlling output of the oscillator shapes are developed from opposite sides of a flip-flop; hence when one gate is "open" the other is shut. Further gating is provided by another Nand gate controlled by a flip flop whose normal mode

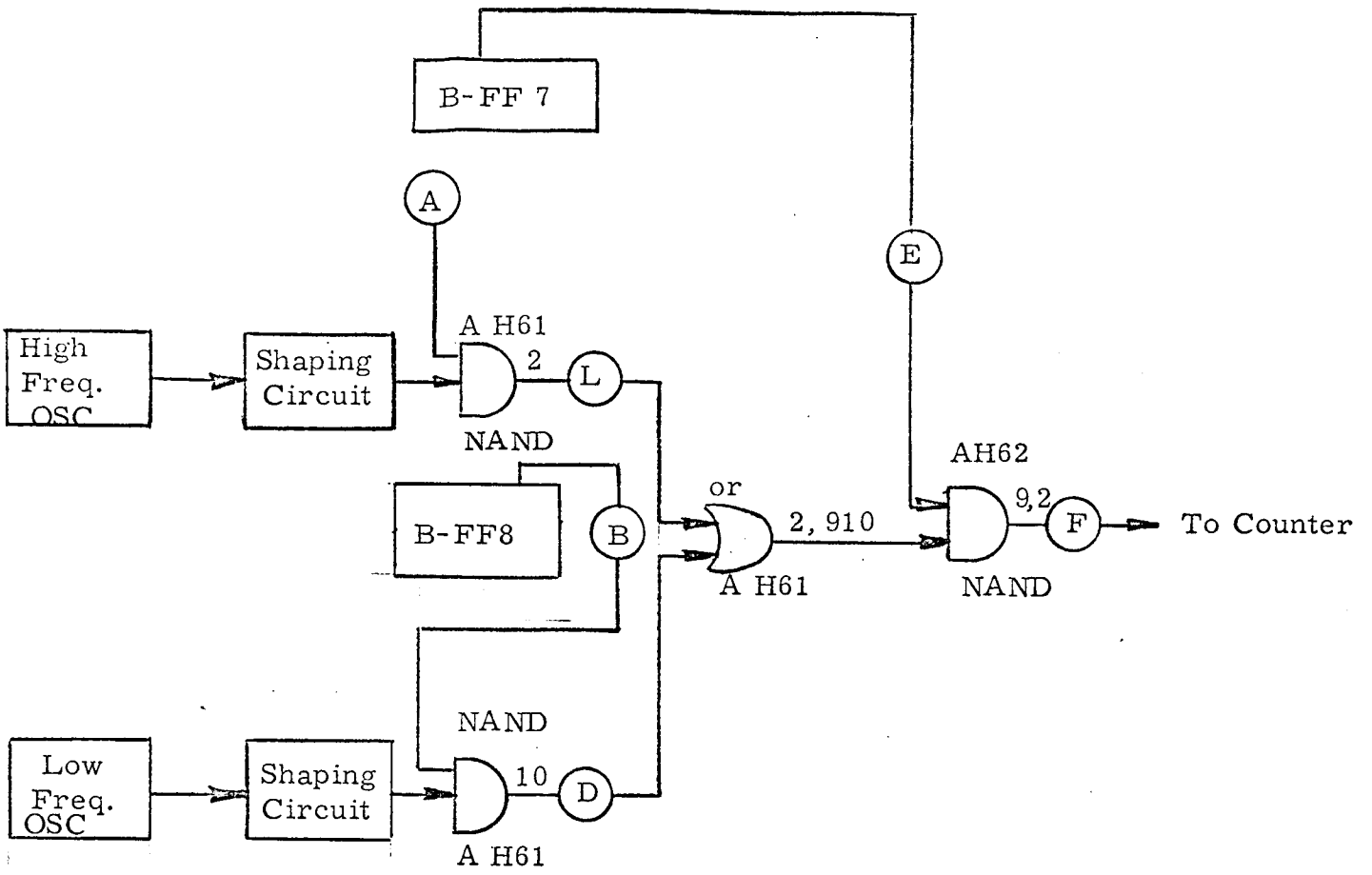


Figure 4.1 A Count Control Circuit

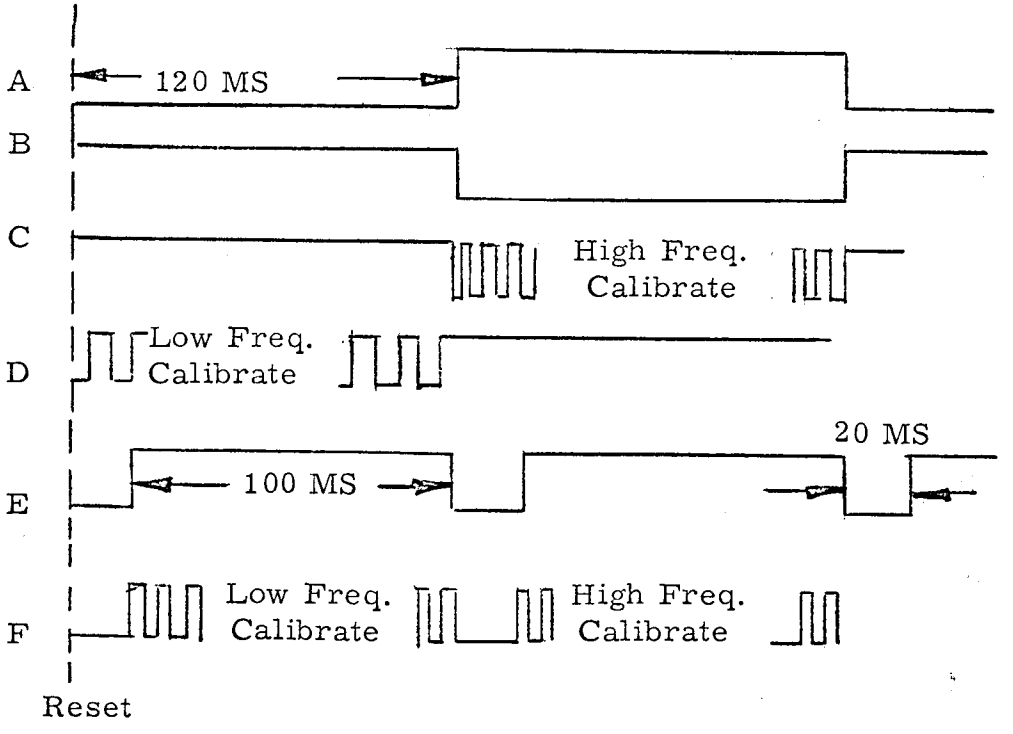


Figure 4.1 B Input & Output to Count Control Circuitry

is disrupted giving the output (signal E) as shown in figure 4.1B. It is this gate and its control which provides the 20 millisecond delay in which the transfer and reset pulses are generated. The output of the last Nand gate goes directly to the counter with no interface circuitry.

4.4.2 Transfer Pulse

5 milliseconds after the start of the 20 millisecond delay of oscillator information to the counter, the transfer pulse is generaged. The associated circuitry for the generator is shown in figure 4.2A. At this point it should be noted that signal E of figure 4.1B is signal A in this presentation, being developed from C-FF7. The flip flop counter circuitry B-FF12, 13 and 14 is being driven from this signal, and in effect count the number of times this signal appears at the input. As long as signals D and F are down (low), Nand gate B-G4/9 will pass the pulse generated by signal E. Signal E is passed through one shot mutivibrator having a pulse duration of approximately 11 usec. Before going to the transfer gate it is passed through an inverter for logic compatibility. Like C-FF7, the flip flop C-FF10 is a binary frequency divider which has had its regular output modified; the method of accomplishing this will be shown later.

4.4.3 Relay Driver Pulse

The method of generating the relay driver pulses are also shown in figure 4.2A. The 3 flip flop binary counter which drives Nand gate B-G4/8 also drives 2 additional Nand gates. The output of these gates go directly to the

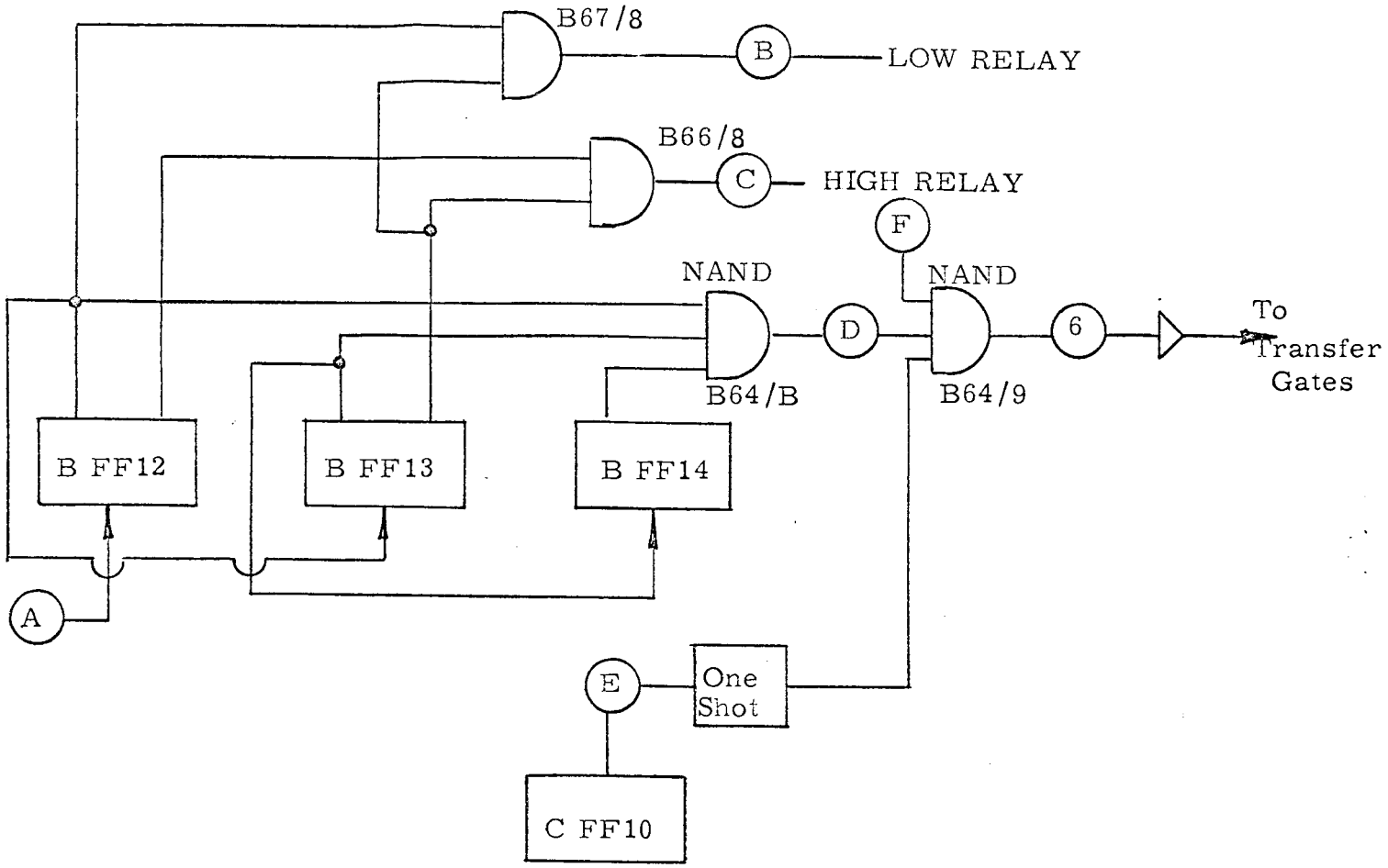


Figure A. Relay Driver and Transfer Pulse Circuitry

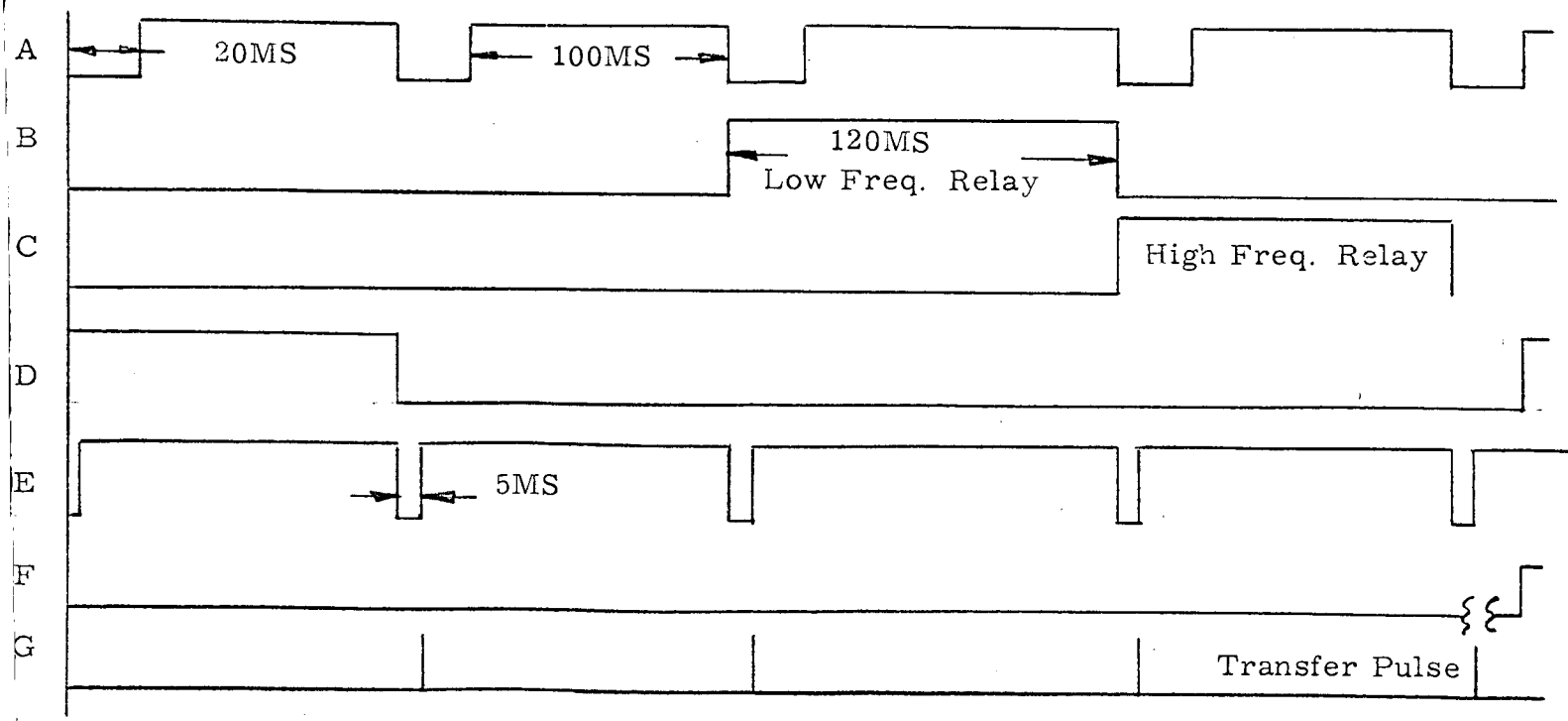


Figure 4.2B. Timing Pulses for Relay Drivers and Transfer Pulses

inputs of the relay driver. Hence when the carry side of BFF12 and BFF13 are high there is an output from Nand-gate B G6/8 which will energize the high frequency relay driver. The output sequency of these gates is shown in figure 4.2B.

4.4.4 Reset Pulse

As mentioned previously the read command is really a reset pulse, reseting the entire instrument. The counter on the other hand can be reset periodically from internal circuitry as shown in figure 4.3A. Because the reset signal to the shift register is a DC level rather than a pulse the R-C integrating interface circuitry shown is to present stray pulses from perhaps accidently reseting a portion or stage of the shift register.

The binary frequency divider flip flop C-FF9 has had its normal mode interrupted similar to CFF7 and CFF10; its output is shown in figure 4.3B. The output of this flip flop, sent through a non-inverting one-shot multivibrator with a pulse duration of approximately 11 usec., forms the counter reset pulse which occurs during the 20 millisecond delay of oscillator information to the counter. Signal C of figure 4.3B is not used in the generation of the counter reset pulse, but is included only to show the occurance of the reset pulse in reference to it.

The dual inverters driving the first two stages of the counter are only for logic compatibility for the high frequency stages as previously explained.

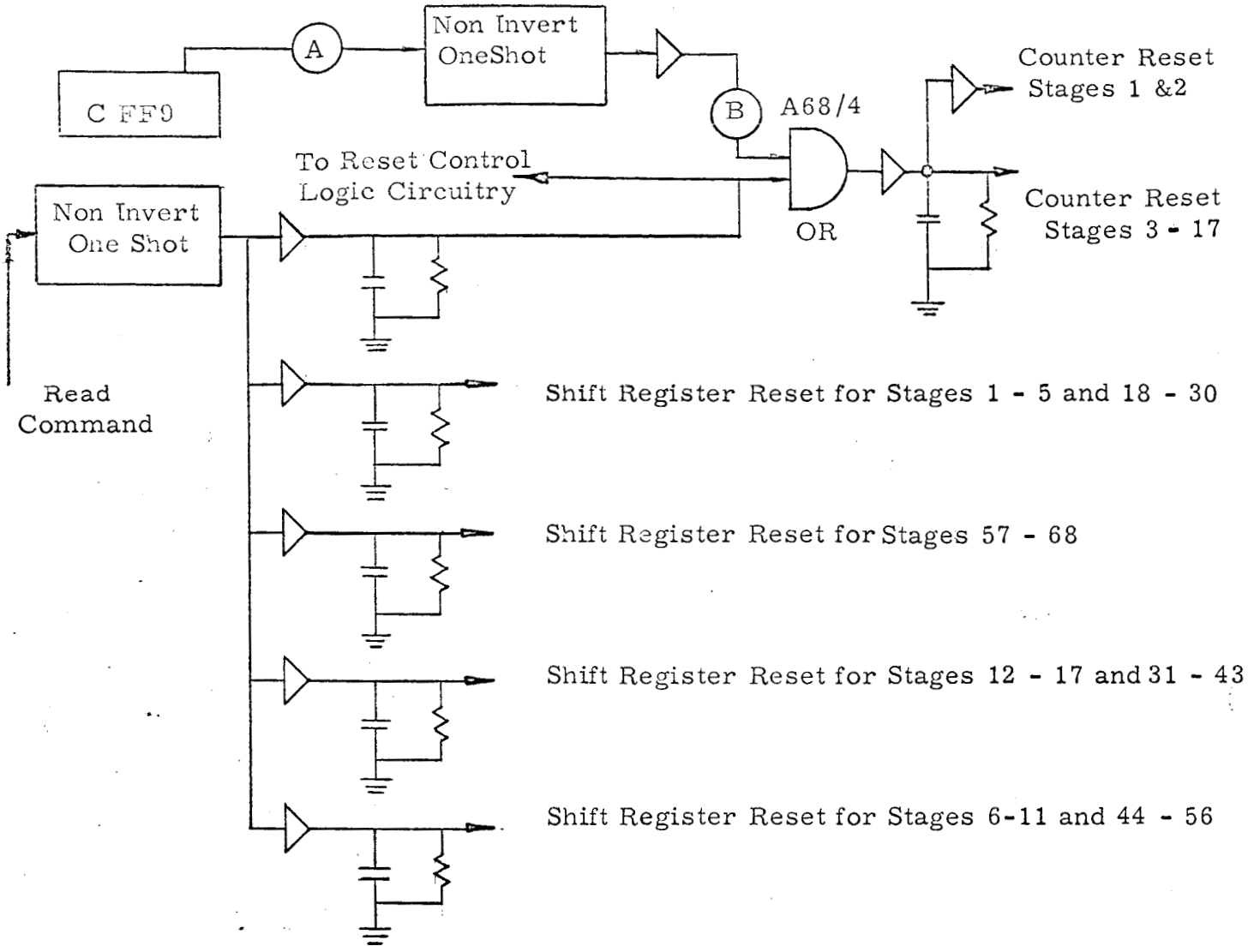


Figure A. Counter and Shift Register Reset Circuitry

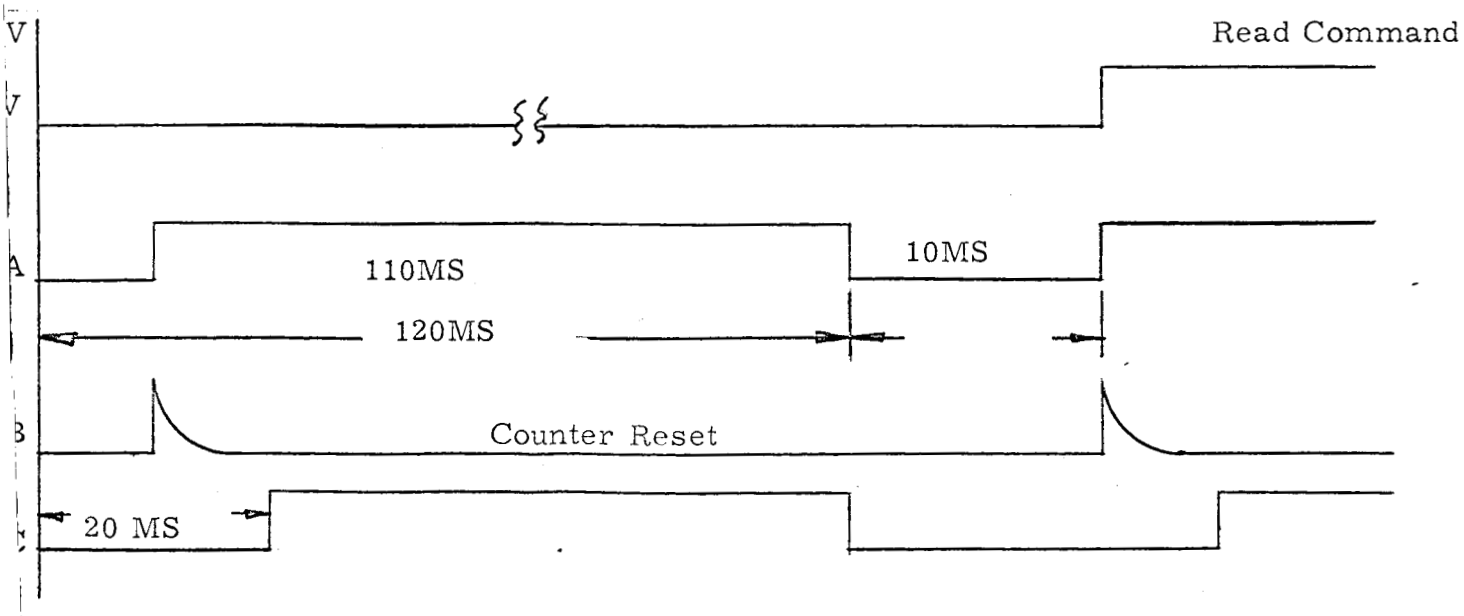


Figure 4.3B. Read Command and Counter Reset Pulses

4.4.5 Shift Pulse Circuitry

The shift pulses to the register occur at two rates; 17 pulses at the rate of 200 per second after each transfer pulse lasting for 82.5 millisecond, and 68 pulses occuring at the rate of 400 pulses per second gated in coincidence with the shift command, lasting for 168.75 millisecond for read out to telemetry. The circuitry and signals generating these pulses are shown in figure 4.4A and B respectively.

The 68 shift pulses occur whenever the shift command opens Nand Gate C-G3/4 allowing the 400 cycle clock to be applied to the shift pulse lines. The 17 shift pulses are generated internally yet derived from the 400 cps clock pulse. As long as signals G and H are such that Nand gate C-G2/8 is open the shift pulses actually are the pulses coming from C-FF1, which is a binary frequency divider being driven from the 400 cps clock pulses; hence the output of this flip flop is at the rate of 200 cps.

The read command will reset B-FF11 such that signal H would open Nand gate C-G2/8, and this signal will not change until 4 sets of 17 shift pulses have been applied to the shift register. Actually B-FF14 will set BFF11 after counting 4 input signals from C-FF7.

This then leaves signal G, which is gated by signals D & E as the largest controlling factor of gate C-G2/8. Signal E is dependent upon the same as signal A. Signal D on the other hand is generated from a divide by three circuit which is "up" once for every 3 times signal C is up. The output

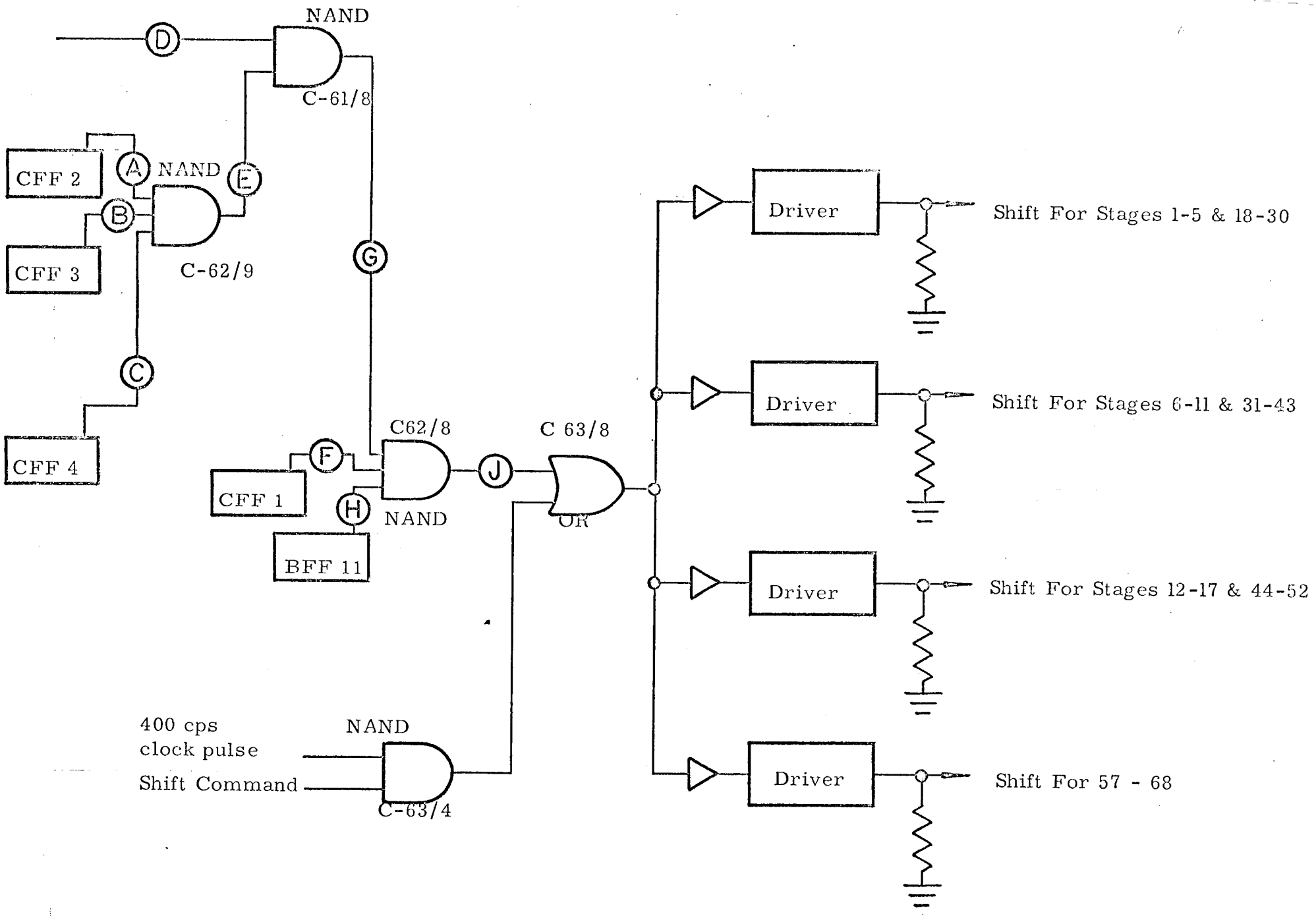


Figure 4.4A Control And Development Of Shift Pulses

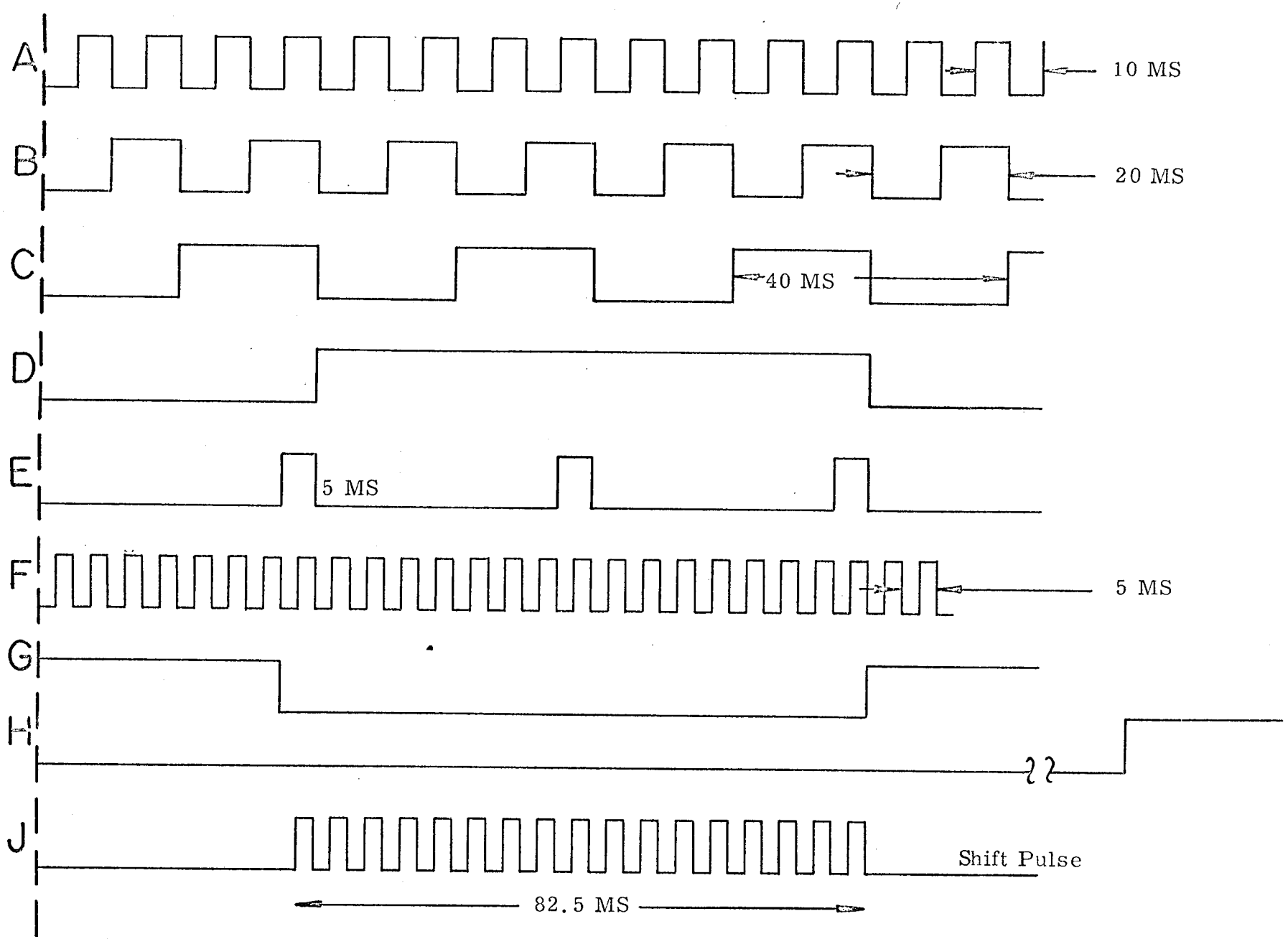


Figure 4.4B Input And Output Signals To Control Shift Pulses

of Nand gate C-G1/8 will be up, thereby shutting off Nand gate C-G2/8, anytime signals D and E are both down. Whenever either or both signals D and E are up however, signal G will be down, and until signal H changes will open Nand gate C-G2/8 to pass the output of C-FF1.

The clock drivers in the shift pulse lines are present to insure sufficient drive capabilities to all 68 stages of the register, since each driver is only capable of driving 20 stages.

4.5 DEVELOPMENT OF CONTROL SIGNALS

The circuitry necessary to develop the proper control signals to be applied to the control gates is shown in figure 4.5 A, while the outputs of each stage is shown in figure 4.5B. All ten flip flops used in this circuitry are basically of the RST type. While each flip flip has the capability of its regular outputs, that is Q and $\bar{Q}$, they also have additional capability of those outputs from a low impedance emitter follower. In the interest of simplicity however only one side of the outputs have been shown in figure .

The first stage is driven by the spacecraft 400 cps clock pulse; signal labled A. All ten stages are reset by the arrival of the read command pulse to the reset input. Each of the first four stages act as a standard ripple through divide by two binary counter stage. The second stage while driving the T input of the third stage also applies its output to the set input of the tenth stage. Similarily the output of the 3rd stage drives the T input of the fourth stage and in addition provides an input to the set input of the ninth stage. The fifth and

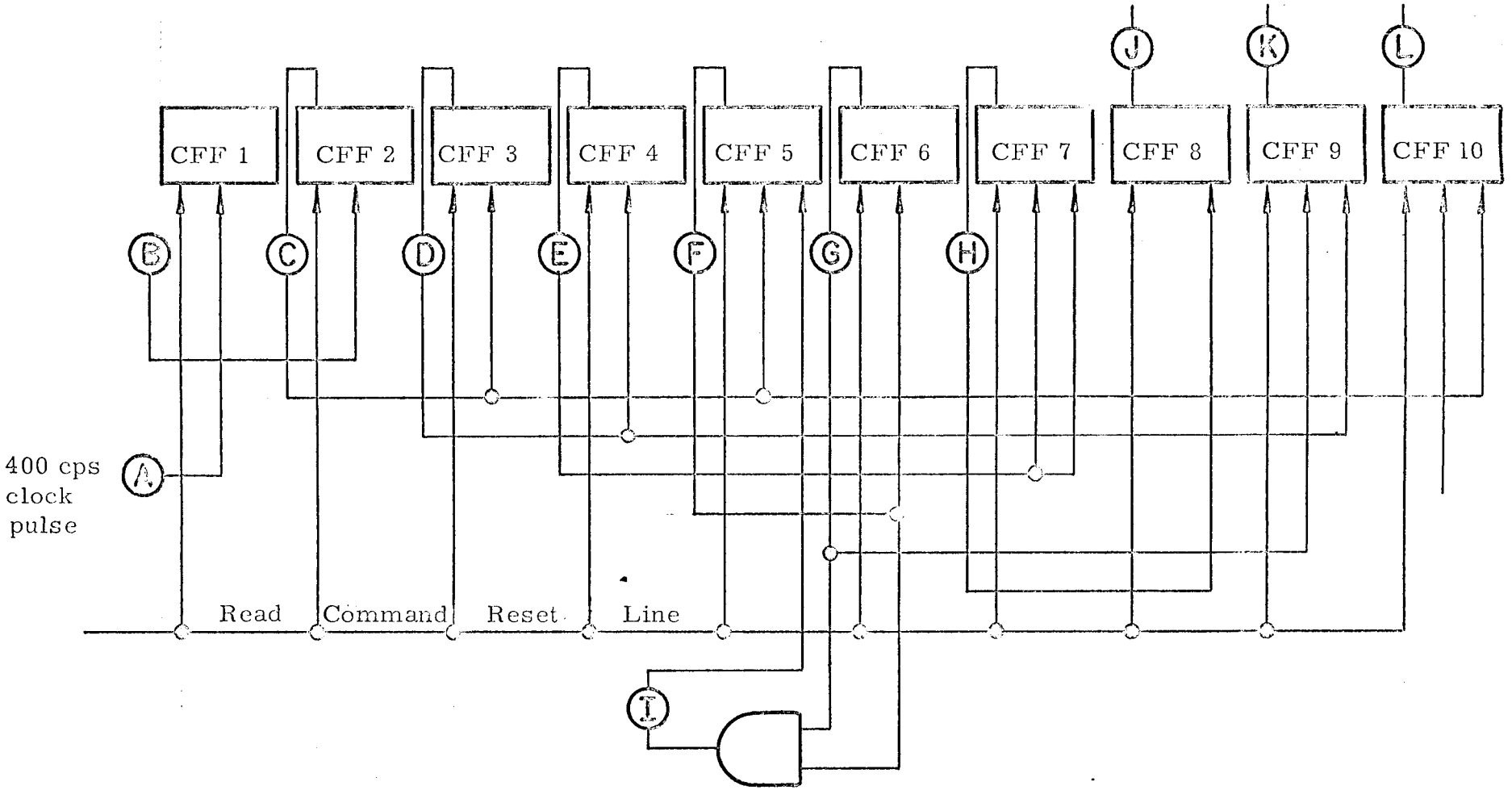


Figure 4.5A Control Signal Development Circuitry

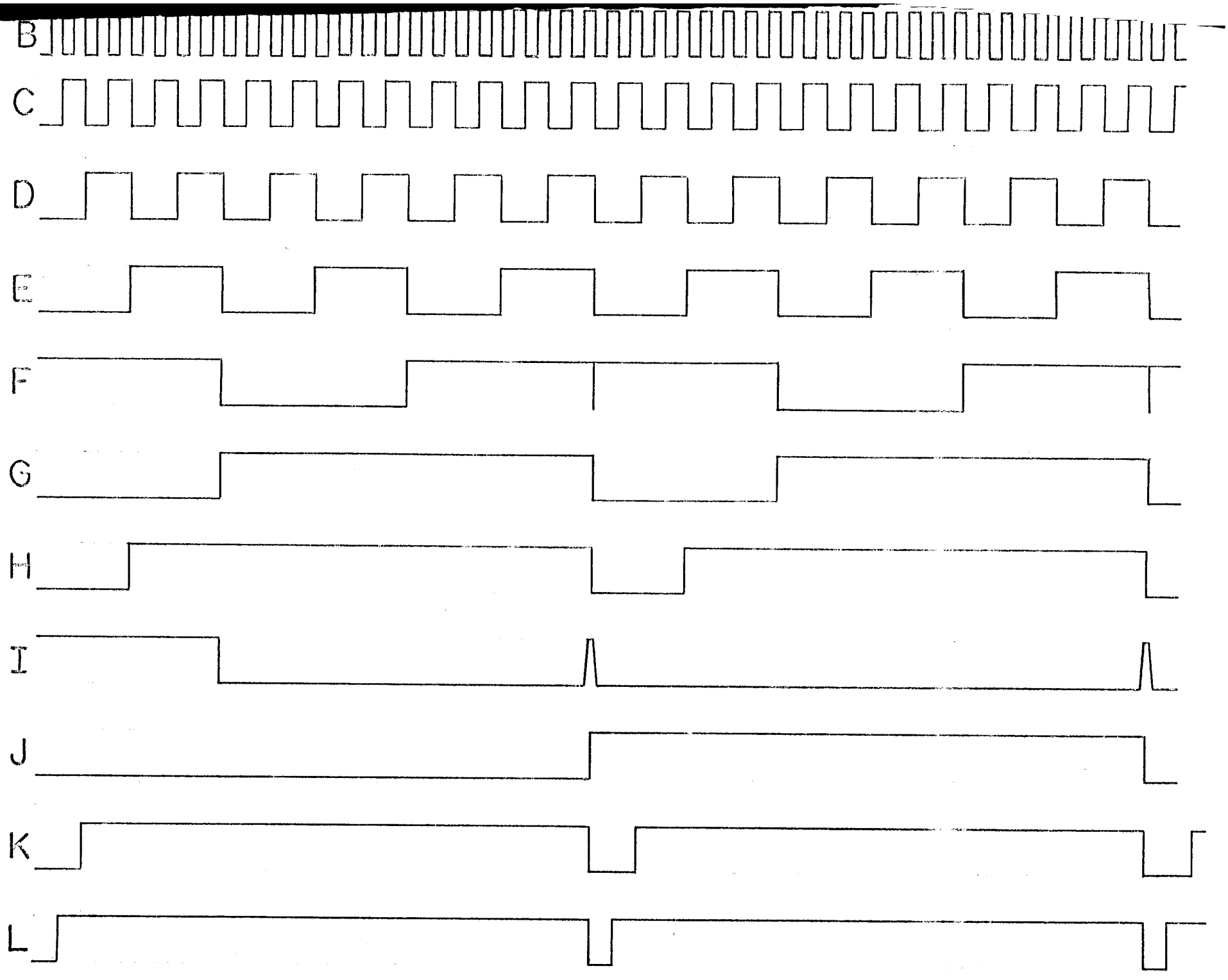


Figure 4.5B Signals Developed For Control Circuitry

sixth stages together with the associated Nand gate provide a divide-by-three circuit; the output of the sixth stage driving the T inputs of the seventh, ninth and tenth stages.

4.6 RELAY DRIVER OPERATION

Because the low frequency oscillator relay pulls in first, the relay driver will be described in terms of this driver, however both relay drivers are identical. The circuitry for these drives are shown in the overall schematic.

Before the arrival of the actuating pulse the base of Q_3 is at ground potential. Thus forward biasing this emitter follower; hence at full saturation approximately one-half volt is developed across it. Because of the low positive voltage at the junction of the 3.9K ohm and 1.5K ohm resistors the base of Q_4 is biased off at approximately -5 volts, hence the relay is de-energized.

With the arrival of a positve 3.5 volt pulse to the base of Q_3 the bias on the PNP transistor Q_3 is now such as to apply reverse bias to the base-to-emitter junction, thereby cutting off this stage. With the emitter follow cut-off the base potential of the NPN Q_4 becomes positive, putting this transistor into full saturation, and the appropriate relay will be energized thus switching the appropriate oscillator from the calibrate capacitor to the antenna and its capacitance.

The positive pulse (+3.5V) which is sent to the relay drivers will last for 120 millisecond and is developed from the control logic circuitry. As can be seen from Figure 4.2B during the first two 120 millisecond periods the

Capacitance Probe is on and neither relay is energized, then the low frequency is energized for the 3rd 120 millisecond intervals upon completion of which the low frequency relay is again de-energized and the high frequency relay driver is energized for 120 milliseconds during the 4th interval.

4.7 OSCILLATOR CIRCUIT

The oscillator circuit is shown in figure 4. 6A, while the AC equivalent circuit for this oscillator is shown in figure4. 6B. Both the high and low frequency oscillator circuits are identical with the exception of some values of resistors, capacitors and the baluns; thus the description will be made in terms of the high frequency circuit. The calibration frequencies are one megocycle for the high frequency and 750 kc for the low frequency oscillator.

Resistors R33, R34, R35 and R36 determine the bias point and hence the quiescent operating point of transistor Q_7. Similarly for the emitter follower resistors R37, R38, R39 and R40 determine the quiscent point for Q_8. The oscillator output signal is developed across R36, the emitter AC load resistor and coupled through C18 to the emitter follower buffer stage.

The operation of the oscillator is more simply seen if the parallel capacitors are grouped into one equivalent capacitance as shown in figure 4. 6B. The signal developed across R36 is fed back to the junction of C_2 and C_3 sustaining oscillations at the frequency determined by L_1', C_1', C_2', C_3' and the reflected capacitance from the primary of the transformer. Capacitors C_{16} and C_{17} offer

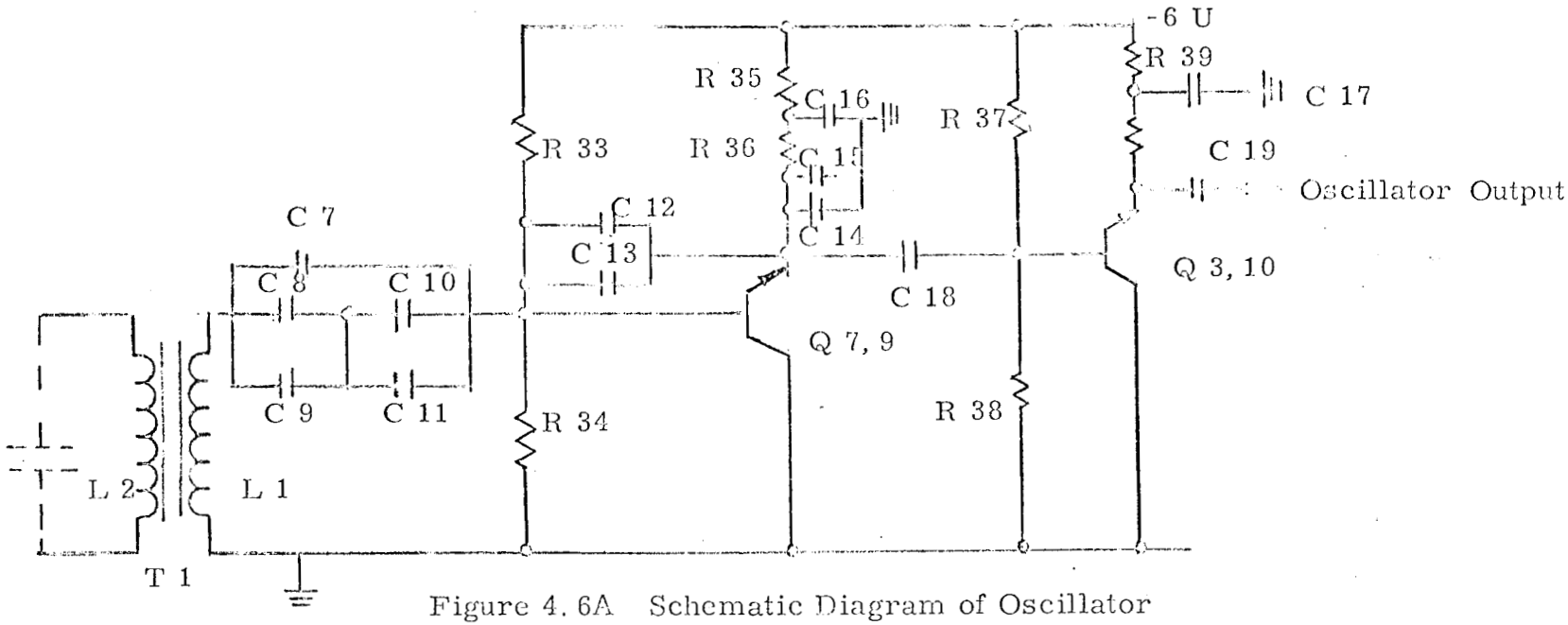


Figure 4.6A Schematic Diagram of Oscillator

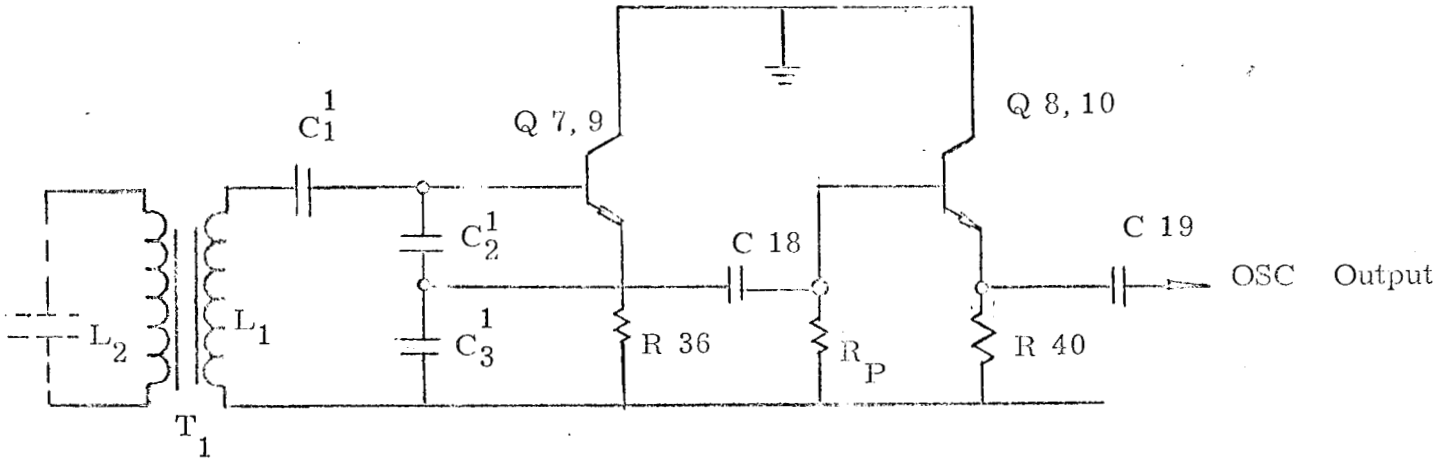


Figure 4.6B. A.C. Equivalent Circuit of Oscillator

a low impedance path for AC thereby effectively grounding R35 and R39 hence the AC load impedance is R36 and R40 for each stage.

4.8 LIMITING AND SQUARING CIRCUIT

The output of each oscillator is fed to separate squaring circuitry, both of which are identical; this circuitry is shown in figure 4.7A. The output of the oscillators are sinusoidal, however, to be fed to the counter the waveform must be squared, or formed into pulses which can be counted by the conventional ripple through binary counter.

The 10K ohm resistor at the input to the schmitt trigger serves as a isolation resistance and also forms part of the gain relationship for the Fairchild F-710C Amplifier. The ratio of the 200K ohm feedback resistor to the 10K ohm input resistance determines the gain of the amplifier, which is 20. The diodes at the input to the Fairchild amplifier will limit the sinewave input to approximately $\pm$ .6 volts to prevent damage to the amplifier.

Since the input signal to the F-710 amplifier is fed to the inverting input, as the input signal goes positive, the output will go negative and because of the gain, the amplifier will go into saturation, giving a -3 volt output until the input signal again goes through zero whereupon the output is again saturated in the opposite direction to +3 volts. The 10K resistor from the non-inverting input (+) of the Fairchild F-710C amplifier to ground is selected so that both inputs to the amplifier will see the same impedance. The signal has now been transformed from a sinewave to a square wave of the same frequency.

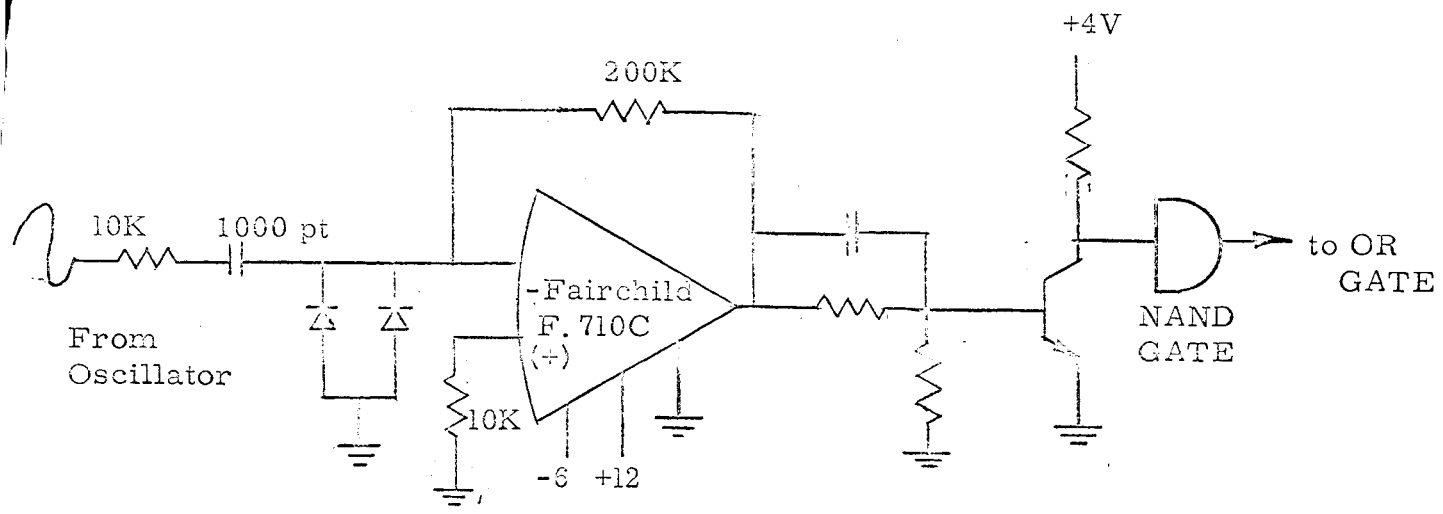


Figure 4.7 Limiting And Squaring Circuit

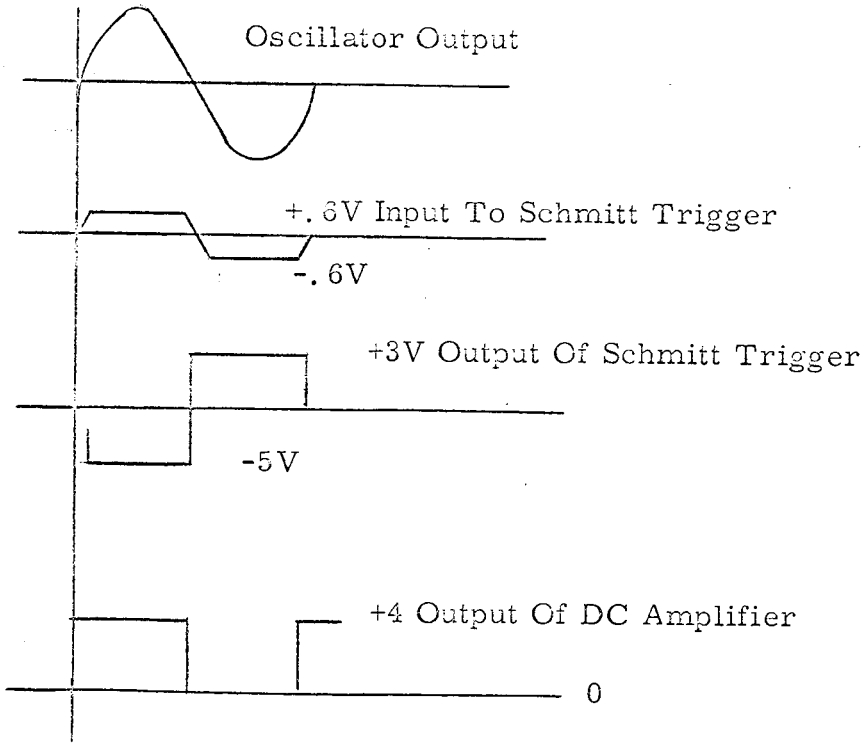


Figure 4.7B Waveforms Of Limiting And Squaring Circuit

The NPN transistor amplifier following the schmitt trigger is used mainly to change the level of the square wave shifting from +4 volts to ground, so that the square wave is compatible to drive the A HG1 Nand gate. When the input to this stage is negative the transistor Q is cut off and the output to the Nand gate is + 4 volts. However, when the input becomes positive the base to emitter becomes forward biased causing the transistor to conduct hard and the output to the Nand gate approaches ground.

4.9 OUTPUT BUFFER AND LEVEL SHIFTER

The output of the 68th stage of the shift register goes to the input of the first stage by trigger steering previously explained, and the output is also to telemetry through a buffer and level shifter stage as seen in the overall schematic.

With the output of the 68th stage at ground potential transistor Q_{13} is cut-off with approximately -. 64 volts of back bias applied to the base. This means that the base of Q_{14} is forward biased and this stage is in hard conduction, hence approximately 4. 35 volts would be applied across R 76; thus the output is following the input minus V BE. The diode, CR8, prevents more than . 6V reverse bias to be applied to transistor Q_{14} and also any capacitance discharge loading from the output is fed through the diode and then through the low impedance saturated transistor.

When the positive pulse arrives at the input, Q_{13} becomes forward biased and conduts, placing the junction of R74 and R75 very close to ground

Now Q_{14} is cut-off and the output zero. Again, should there be any capacitance loading try to discharge through R76 the diode would reduce the impedance with a parallel path. The output voltage levels to telemetry then are ground and 4.3 volts.

V. RELIABILITY AND FAILURE ANALYSIS

5.1 SUMMARY

In accordance with specifications, a reliability analysis of the Antenna Capacitance Probe has been conducted. The specifications require a probability of complete success of at least 0.8 and a probability of complete failure not greater than 0.05. The reliability analysis indicates a probability of complete success of 0.94937 and a probability of complete failure of 0.044012.

5.2 GUIDELINES FOR ANALYSIS

As suggested by the Military Standardization Handbook "Reliability Stress and Failure Rate Data for Electronic Equipment," MIL-HDBK-217, this analysis assumes that the reliability of complex electronic equipment depends primarily upon the reliability of the parts used in the equipment. The part failure rate is the parameter on which the estimate is made. The part failure rates given in MIL-HDBK-217 are primarily applicable to standard parts subjected to electrical stresses between 0.1 (10%) and 1.0 (100%) of their rated values. Failure data relative to stresses below 0.1 were either statistically insignificant or indicated that 0.1 was the threshold below which little or no reduction in failure rate could be anticipated.

Although a complete reliability analysis should include both catastrophic (random) and performance degradation failures, most degradation failures are eliminated through conservative design. Therefore, equipment failure is

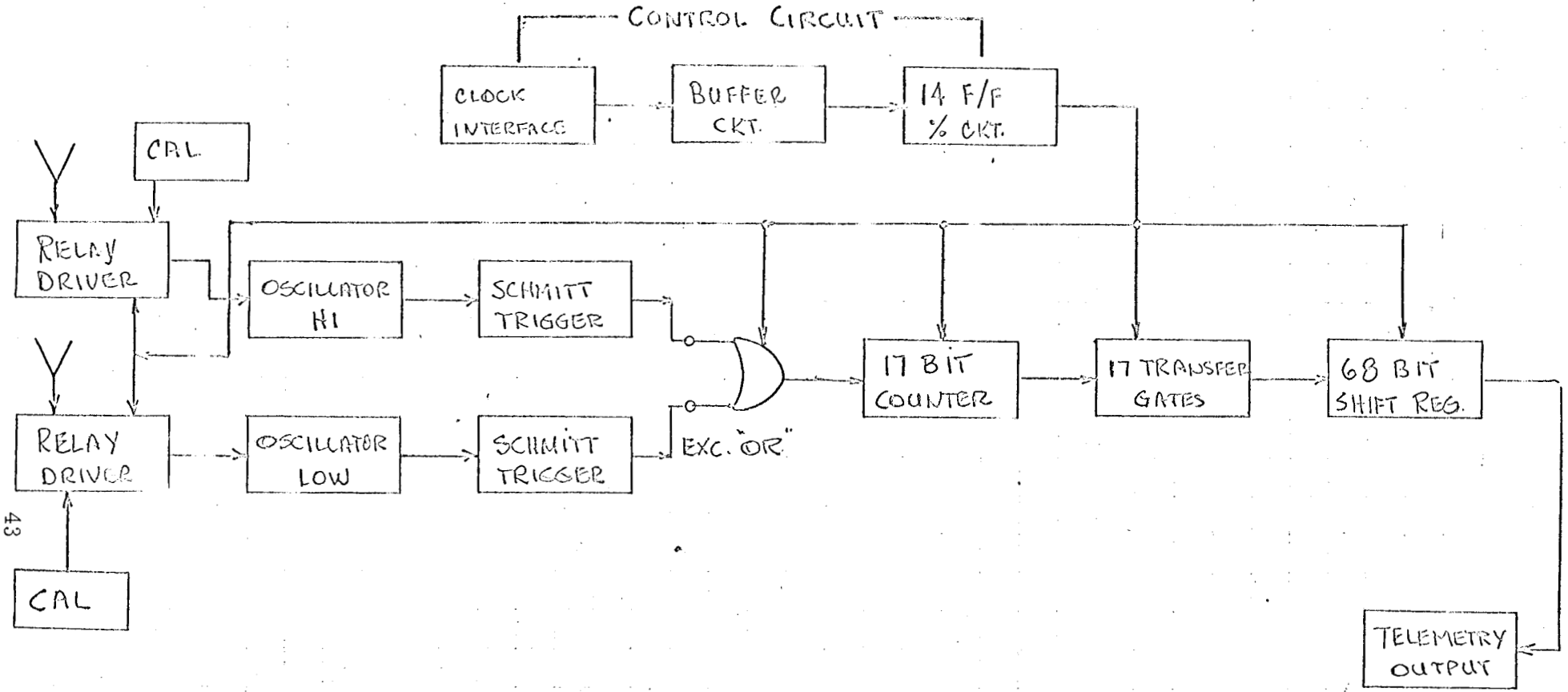
primarily dependent upon the number of catastrophic failures that occur as a function of time.

The following reliability report covers the Radio Astronomy Experiment and the procedure for this report is based on the following assumptions: (a) any failure that occurs will be considered a catastrophic failure; (b) catastrophic part failures occur randomly and exhibit a constant failure rate; (c) all component failures are to be considered catastrophic failures with certain exceptions.

5.3 SYSTEM RELIABILITY

The system reliability shall be computed on the basis of using most recent, manufactures reliability reports and MIL HDBR 217 to establish those reliability data not available from manufacturers specifications.

The system under consideration is shown in Figure 5. 1. All components are operated at less than 50% of their rated maximum operational specifications. The system can be considered a complete failure if the nexus between input and output is broken due to an open or short failure. The control circuit is not part of the series path for data flow however, its prime function is to give the data to the output and therefore a failure in this function is catastrophic.



System Block Diagram

Figure 5.1

Circuit Tabulation:

"17 Bit Counter"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
SN 5112	TI	15	0.016%/1000HR*	0.24%/1000HR
SE 1243	Signetics	2	0.04%/1000HR**	0.08%/1000HR
				0.32%/1000HR

"Transfer Gates"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
SN 5161	TI	5	0.016%/1000HR	0.08%/1000HR
SN 516A	TI	1	0.016%/1000HR	0.016%/1000HR
				0.096%/1000HR

"Shift Register"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
SN 5111	TI	17	0.016%/1000HR	0.272%/1000HR
SN 510	TI	51	0.016%/1000HR	0.816%/1000HR
				1.088%/1000HR

** All Signetics failure data based on interpolated data taken from Signetics memo "Present Reliability Status" 28 February 1964. 60% CL at 55°C

* All TI Failure report data obtained from 1964 supplement to 1963 Failure Report and is established for 60% CL at 55° C.

"Control Circuit"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
SN 511 A	TI	9	0.016%/1000HR	0.144%/1000HR
SN 5111	TI	5	0.016%/1000HR	0.080%/1000HR
SN 518A	TI	3	0.016%/1000HR	0.048%/1000HR
SN 517A	TI	4	0.016%/1000HR	0.064%/1000HR
SN 514A	TI	2	0.016%/1000HR	0.032%/1000HR
SN 513 A	TI	8	0.016%/1000HR	0.128%/1000HR
Transistor 2N929	TI	2	0.020%/1000HR	0.040%/1000HR
Resistor	Welwyn	15	0.001%/1000HR	0.015%/1000HR
Capicator MC80	Aerovox	9	0.001%/1000HR	0.009%/1000HR
				0.560%/1000HR

"Exclusive Or Gate"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failture Rate
SE 115G	Signetics	2	0.04%/1000HR	0.08%/1000HR
				0.08%/1000HR

"Schmitt Trigger"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
F 710 IC	FCHD	1	0.020%/1000HR	0.020%/1000HR
Transistor 2N929	TI	1	0.020%/1000HR	0.020%/1000HR
Diode 1N916	FCHD	2	0.010%/1000HR	0.020%/1000HR
Capicator MC 80	Aerovox	2	0.001%/1000HR	0.002%/1000HR
Resistor F-25 1/4W	Welwyn	6	0.001%/1000HR	0.006%/1000HR
				.068%/1000HR

"Relay Driver"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
Transistor 2N 871	FCHD	2	0.020%/1000HR	0.040%/1000HR
Diode 1N916	FCHD	1	0.010%/1000HR	0.010%/1000HR
Relay BRJ12C1P6AS	Filtors	1	0.011%/1000HR	0.011%/1000HR
Resistor F-25 1/4W	Welwyn	3	0.001%/1000HR	0.003%/1000HR
				0.064%/1000HR

"Oscillator"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
Transistor 2N 915	TI	2	0.020%/1000HR	0.040%/1000HR
Transformer	WTA	1	0.050%/1000HR	0.050%/1000HR
Capicator DM 15	ARCO	13	0.001%/1000HR	0.013%/1000HR
Resistor F-25 1/4W	Welwyn	8	0.001%/1000HR	0.008%/1000HR
				0.111%/1000HR

"Calibrate Network"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
Capicator DM 15	ARCO	2	0.001%/1000HR	0.002%/1000HR
				0.002%/1000HR

"Telemetry Output"

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
Transistor 2N930	TI	2	0.020%/1000HR	0.040%/1000HR
Diode 1N916	FCHD	1	0.010%/1000HR	0.010%/1000HR
Capicator DM 15	ARCO	1	0.001%/1000HR	0.001%/1000HR
Resistor F-25 1/4W	Welwyn	6	0.001%/1000HR	0.006%/1000HR
				.057%/1000HR

Miscellaneous

Component Type	Manufacturer	Quantity	Failure Rate	Total Failure Rate
Filter Capicator (Tantalum)	Sprague	8	0.012%/1000HR	0.096%/1000HR
Connectors	Cannon	2-1a	0.011%/1000HR	0.011%/1000HR
		1a	0.004%/1000HR	0.004%/1000HR
				0.021%/1000HR

$$\lambda_T = \sum_{i=1}^{i=N} \lambda i + \lambda i+1 \ldots\ldots \lambda_N$$

λ_i = Part Failure Rate (%/1000HR)

λ_T = Composite Failure Rate for the Part Group Under Study

Item		Total Failure Rate (%/1000HR)
17 Bit Counter		0.32
Transfer Gates		0.096
Shift Register		1.008
Control Circuit		0.560
Exclusive Or Gate		0.080
Schmitt Trigger	2 a 0.068	.136
Relay Driver	2 a 0.064	0.128
Oscillator	2 a 0.111	0.222
Calibrate Network	2 a 0.002	0.004
Telemetry Network		0.057
		2.611 %/1000HRS

λ_T = 2.611 - The total is in accordance with a 60% confidence level and TA= +55°C (Max. thermal stress)

The probability of complete success of the entire Experiment Package:

$$P_s = e^{-\lambda_T t}$$

where t = total operating time

t = 2000 HRS

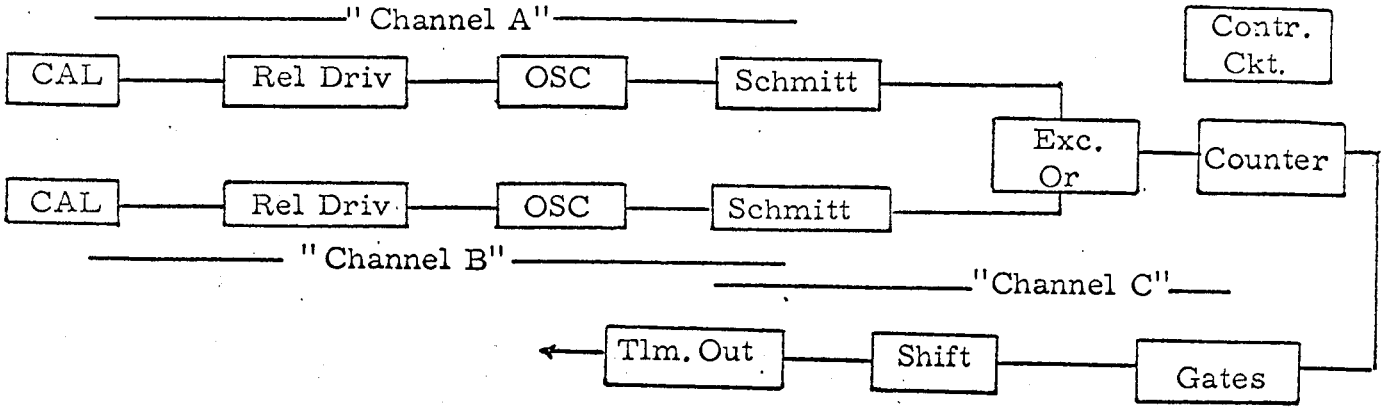
$\therefore$ $P_s = e^{-(2.611\%/1000HRS)(2000\ HRS)}$

$P_s = 0.94937$

Mean Time Between Failure $MTBF = \frac{1}{\lambda_T} = 38.250 \times 10^3$ HRS

P s including 400 hrs. test time = 0.93950

Probability of Total Failure



Pa = Probability of success of Channel A

Pb = Probability of success of Channel B

Pc = Probability of success of Channel C

Failure Rate of Channel "A"

Cal. Network	.002%/1000HR
Oscillator	.111%/1000HR
Relay Driver	.064%/1000HR
Schmitt Trigger	.068%/1000HR
	.245%/1000HR

$Pa = e^{-.245\%/KHR(2000HR)}$

Pa = 0.99512

Failure Rate of Channel "B"

Pb = Pa = 0.99512

Failure Rate of Channel "C"

17 Bit Counter	0.32%/1000HR
Transfer Gates	0.096%/1000HR
Shift Register	1.008%/1000HR
Control Circuit	0.560%/1000HR
Exclusive Or	0.080%/1000HR
Telemetry Network	0.057%/1000HR
	1.121%/1000HR

$$Pc = e^{-1.121\%/KHR \quad (2000HR)}$$

$$Pc = \frac{1}{1.046} = 0.95602 \qquad P_{c\ Fail} = 1 - Pc = .04398$$

Probability Table

✓ = Criteria for total failure

B = Bad

G = Good

Channel A	Channel B	Channel C
B	G	G
G	G	G
B	B	G ✓
G	B	G
B	G	B ✓
G	G	B ✓
B	B	B ✓
G	B	B ✓

$$Pf = \Big[Pc\ (1-Pa)\ (1-Pb) + Pb\ (1-Pa)\ (1-Pc) + Pa\ Pb\ (1-Pc) + (1-Pa)\ (1-Pb)\ (1-Pc) + Pa\ (1-Pb)\ (1-Pc) \Big]$$

$$Pb = Pa$$

$$Pf = Pc\,(1-Pa)^2 + (Pa-Pa^2)\,(1-Pc) + Pa^2\,(1-Pc) + (1-Pa)^2\,(1-Pc) + (Pa-Pa^2)\,(1-Pc)$$

$$= Pc\,(1-Pa)^2 + 2\,(1-Pc)\,(Pa-Pa^2) + Pa^2\,(1-Pc) + (1-Pa)^2\,(1-Pc)$$

$$= 23.698 \times 10^{-6} + 433.364 \times 10^{-6} + .04355 + 1.0473 \times 10^{-6}$$

$$Pf = 0.044012$$

APPENDIX A
SPECIFICATION FOR ENGINEERING MODEL OF THE CAPACITANCE PROBE

1. SCOPE

The unit supplied will be used in engineering integration tests of the electronic system of the RAE satellite. The purpose of these integration tests in to make possible the writing of an accurate specification for the prototype and flight models of this unit for the satellite. This satellite will be a non-scaled satellite with a circular orbit inclined 50 degrees to the equator at an altitude of 6000 kilometers.

2. APPLICABLE DOCUMENTS

The provisions of the following specifications, standards, drawings and publications of date of current issue will apply as detailed in this specification. In the event of a conflict, the detailed provisions of this specification shall govern.

MSFC Std. 154	Printed circuit design and construction.
MS 33586	Metals, definition of dissimilar electric.
MIL-I-6181D	Interface control requirements, aircraft equipment.
S-320-D1	General environmental test specification for Spacecraft and components.
GSFC TID-S-100	Specification for contractor-prepared monthly, periodic, and final project reports.
GSFC X623-63-147	Specification drawings, engineering and associated lists.

MIL-JDBK-217	Reliability stress and failure rate data for electronic equipment.
GSFC-PPL-3	Preferred parts list.
FED-STD-102	Preservation packaging, and packing levels.
FED-STD-123	Marking for domestic shipment.

2.1 Mechanical Drawings

GB-RAE-1155-001	Standoff
GB-RAE-1155-002	Insulator Board
GB-RAE-1155-003	Spacer
GB-RAE-1155-004	Can
GB-RAE-1155-005	Encapsulation Procedure
GC-RAE-1155-009	Retaining Strip
GC-RAE-1155-011	Rear Panel
GD-RAE-1155-500	Container Cover
GD-RAE-1155-505	Cover
GD-RAE-1155-504	Right Side Panel
GD-RAE-1155-507	Container
GD-RAE-1155-511	Left Side Panel
GF-RAE-1155-512	Capacitance Probe Electronic Enclosure Assembly
GF-RAE-1155-513	Front Panel

2.2 Electrical Drawings

GC-RAE-1155-006	Printed Wiring Assy Control #4
GC-RAE-1154-007	Printed Wiring Board Control #4
GC-RAE-1155-008	Printed Wiring Main Board
GC-RAE-1155-010	Printed Wiring Board Test Limiter
GR-RAE-1155-101	Printed Wiring Assy Shift Register
GD-RAE-1155-203	Welded Module T & R Driver
GD-RAE-1155-204	Printed Wiring Assy Test Limiter
GD-RAE-1155-205	Printed Wiring Assy RAE Oscillator
GR-RAE-1155-206	Schematic Diagram RAE Capacitance Probe Experiment
GD-RAE-1155-402	Printed Wiring Assy Counter Shift Register
GD-RAE-1155-403	Printed Wiring Assy Control #1
GD-RAE-1155-404	Printed Wiring Assy H. S. Counter Shift Register
GD-RAE-1155-405	Printed Wiring Assy Control #2
GD-RAE-1155-406	Printed Wiring Assy Control #3
GD-RAE-1155-501	Printed Wiring Board Control # 3
GD-RAE-1155-502	Printed Wiring Board H. S. Counter Shift Register
GD-RAE-1155-503	Printed Wiring Board Shift Register

GD-RAE-1155-506	Printed Wiring Board Control #2
GD-RAE-1155-508	Printed Wiring Board Control Circuit#1
GD-RAE-1155-509	Printed Wiring Board Counter Shift Register
GD-RAE-1155-510	Printed Wiring Board RAE Oscillator
GR-RAE-1155-514	Printed Wiring Assy Main Wiring

2.3 Other Documents

Report No. NAS 9175-1	Final Report on "Engineering Model of Antenna Capacitance Probe", Part No. 2158-R-434, under Contract No. NAS 5-9175

3.1 REQUIREMENTS

The capacitance probe shall be designed and constructed to satisfy all of the requirements specified herein.

3.1 General

3.1.1 Materials

Materials and processes uded during manufacture of items covered herein shall be of high quality, suitable for the purpose, and conform to applicable government and contractor's specifications whenever possible. Materials and components of proven reliability shall be employed to the greatest practicable extent.

3.1.1.1 Metals

All metals which are used in the construction of the items covered by this specification that are subject to deterioration when exposed to the climate and environmental conditions specified in U. S. Government Spec. S-320-D1 shall be protected in a manner that will in no way prevent compliance with this specification. The use of protective coatings that will crack, chip or scale with age or extremes of climatic and environmental conditions shall be avoided.

Dissimilar metals as defined by MS 33586 shall not be used in intimate contact unless protected against electrolytic corrosion.

3.1.2 Interchangeability

All parts having the same manufacturers parts numbers shall be directly and completely interchangeable with each other with respect to installation and performance, except as approved specifically by the purchaser.

3.1.3 Workmanship

"The units including all parts and accessories shall be manufactured in a thorough workmanlike manner in accordance with best commercial practice. The provisions of MSFC 154, 270, 271 and NPC 200-4 shall be applicable. Component interconnections shall be soldered."

3.2 Electrical Requirements

The capacitance probe shall monitor a dipole antenna in accordance with the operational program of spacecraft and shall develop a signal which indicates the capacitive reactance of the antenna. This isgnal shall be processed and stored in a format which is compatible with the spacecraft telemetry system.

The instrumentation for the antenna capacitance measuring system shall be divided into two packages. One package shall be located near the antennas to be measured and shall contain the capacitance oscillators, the calibration capacitors, and associated switching relays and gates. The main package shall be located in the main body electronics stack and will contain power conversion, counter circuit, transfer gates, shift register, clock frequency conversion logic and control logic.

3.2.1 Antenna Capacitance Oscillator

Two closely coupled oscillators shall be located in the package near the antenna terminstions. These oscillators will operate at 750 kc and 1 mc, respectively. The oscillator design shall be basically LC units with a short term

stability of $\pm$ 0.05% from 2.5 seconds after the application of power until the removal of power. The basic oscillator when connected to the antenna will cause a maximum excitation of 5 volts peak to peak to be applied to the antenna.

The respective oscillators shall assume a calibration frequency of 750 kc and 1 mc when their capacitance standard is switched into the circuit. If the antenna capacitance changes, then the basic oscillator frequency will shift. Therefore, f becomes proportional to c. A DC bias can be applied to the antenna if a desired potential is required between the antenna and the spacecraft.

The oscillators shall assume a calibration frequency of 500 kc when a capacitance standard is switched into the circuit. These calibration circuits shall allow a check to be made on the basic oscillator frequency to determine if a drift is occuring.

Upon command from satellite control circuitry, the oscillators shall be gated with logic gating so that their signals shall pass alternately to the counter circuitry.

3.2.2 Counter

A seventeen stage counter shall be used to count the 4 respective oscillator frequencies, two measuring frequencies and two calibrate frequencies. These seventeen stages shall allow a maximum frequency of one megacycle to be recorded. The counter circuit shall have a sample period of 100 milliseconds.

The basic accuracy of the capacitance measuring system shall be achieved by having a sample period of sufficient time to record the frequency to the desired accuracy and by holding the sampling period very accurately.

3.2.3 Transfer Gates

The transfer gates shall be activated by a control signal at the end of the 100 millisecond sample period. These gates shall transfer the binary information from the counter to the shift register.

3.2.4 Shift Register

The shift register shall be composed of 68 stages which shall allow the storage of four, seventeen bit binary words. After the transfer of each seventeen bits and be ready to accept the next binary word into the register. The shift time shall be less than 100 milliseconds. The four digital words shall be accumulated and stored in the following order: high freqeuncy calibration; low frequency calibration; high frequency; and low frequency.

Upon command from spacecraft control circuitry, the shift register will accept the spacecraft shift pulses so that the data can be transferred serially. The output of the last shift register stage will be monitored by telemetry. The rate of shift out will be 400 bits per second. The output of the last stage will be buffered to conform to interface requiements as specified by GSFC.

The shift register shall be capable of being cycled at speeds up to 250,000 bits/second.

3.2.5 Experiment Clock

The experiment clock shall operate from the basic satellite clock pulse of 400 cps square wave, and the basic sampling time of the instrument shall be derived from this clock, which has a frequency stability of $\pm$ 0.1 percent.

The experiment clock shall provide reset signals for the counter and the shift register. The clock shall provide transfer signals for the transfer gates, commands for the gates which control the counter input, signals to drive the oscillator calibrate relay, and experiment shift pulses to shift each word in the register during the data accumulation cycle.

3.2.6 Control Signals

The unit shall operate in conjunction with the external control signals listed below.

3.2.6.1 Power Control

Power shall be externally switched on and off to the unit so that power shall be available only during operating periods.

3.2.6.2 Accumulate Command

An accumulate command shall be provided to the unit to start the data accumulation cycle. It shall be provided at not less than 2.5 seconds after power is provided to the unit.

3.2.6.3 Clock Pulses

Clock pulses shall be provided to the unit as discussed in paragraph 3.2.5.

3.2.7 Accuracy

The overall accuracy of the instrument shall be $\pm$ 0.15 percent or better, including the basic satellite clock error.

3.2.8 Power

The unit shall operate from +6 vdc, -6 vdc, and +3 vdc. These voltages are regulated to ± 1% maximum power consumption shall not exceed the values given below.

+6 volts 40 MA	0.24 watt
-6 volts 20 MA	0.12 watt
+3 volts 300 MA	0.90 watt
Total Power Dissipation	1.36 watt

Not more than 1.36 watts shall be dissipated by the unit for a period of 3.6 seconds every 10 minutes.

3.2.9 Equipment Grounds

Power supply and signal returns shall be isolated from each other and from the case.

3.1.10 Telemetry

The unit shall be suitable for operation with a PCM telemetry system at a rate of 400 to 800 bits per second.

3.3 Mechanical Requirements

3.3.1 Configuration

The instrument shall be packaged in two sections. The main body shall be a standard RAE instrument can 5 x 7 inches with a height of 1-1/4 inches. The other package to be located at the antenna base shall not exceed 9 cubic inches. The actual shape shall be specified by GSFC.

3.3.2 Weight

The total weight of this unit shall not exceed 1.75 pounds. Reduction in weight shall be a prime design consideration.

3.3.3 Packaging

The unit shall be packaged modularly using either printed circuit board or welded module techniques. Two contacts shall be provided on the power supply connector (s) for each power supply connection. All exterior surfaces shall be protected from the environment specified.

3.3.4 Marking

The marking must not deface or damage the equipment or affect its functional use. The marking should be legible with the item mounted in normal position. Each item shall be legibly marked with the following information as a minimum.

Specification Number including latest Revision Number

Part Number and Name

Serial Number

Date of Manufacture (month and year)

Contractor's name and trademark

This information shall preferably be applied to a nameplate (or tag on items too small for a nameplate) securely fastened to the item. It may be applied directly to the surface of the item by acid or electric etching, engraving, silk screen process branding, embossing, casting, molding or by the metal-cal process. The permanency of the marking shall be sufficient to withstand the environmnetal conditions specified. Decals and stencils are not acceptable.

3.4 Environmental Requirements

The unit shall meet all electrical and mechanical specifications throughout the range of environmental conditions specified in this section.

3.4.1 Altitude

The unit shall be capable of operation at a pressure of 10^{-13} torr. Hermetic sealing of parts and assemblies shall be provided to the extent required.

3.4.2 Temperature

The operating temperature range shall be -20° C to $+70^{\circ}$C, and the highest rate of temperature cycling from one extreme to the other shall be 15 minutes. The storage temperature range shall be -30° C to $+70^{\circ}$C.

3.4.3 Humidity

The unit shall operate relative humidity range of 0 to 98 percent.

3.4.4 Vibration

The unit shall meet the sinusoidal and random vibration levels as specified in paragraph 4.2.2.

3.4.5 Acceleration

The unit shall meet the acceleration levels as specified in paragraph 4.3.5 of specification S-320-D-1.

3.4.6 Thermal-Vacuum

The equipment shall operate within specification while exposed to 10^{-13} torr over the range of -20° C to $+70^{\circ}$C.

3.4.7 Radio Frequency Interference

The unit shall conform to the following:

3.4.7.1 Generation

a) Radio Frequency Conducted

The equipment shall be designed to meet the requirements specified in MIL-I-6181D para. 4.3.1 in the frequency range 0.15 to 25 Mc.

b) Low Frequency Conducted

Interface voltages and currents in the frequency range 35 cps to 150 kc in excess of 30 mv and 10 ma peak-to-peak shall not appear on any conductor external to the equipment, which could conduct interference to other equipment.

c) Radiated

Equipment is to meet the requirements specified in MIL-I-6181D para. 4.3.2 in the frequency range 0.15 to 200 Mc.

3.4.7.2 Susceptibility

a) Radio Frequency Conducted

Equipment is to meet the requirements specified in para. 4.3.4.1.1 of MIL-I-6181D. Tests shall be made over 0.15 to 400Mc.

b) Audio Frequency Conducted

No change in indication, malfunction or degradation of performance shall be produced in any equipment when a sine wave signal of 100 mv rms or when a step function or low frequency square wave of 300 mv amplitude having a rise time of less than 1 microsec is applied as shown in Fig. 19 of MIL-I-6181D. Tests shall be made over the frequency range 35 cps to 150 kc.

in performance) during a mission of 10,000 hours (2,000 hours operating time) greater than 0.8 (confidence level 60 percent). Both of these figures refer to operation in the space environment.

4. SAMPLING, INSPECTION, AND TEST PROCEDURES

4.1 Quality Assurance

The contractor shall conform to specification NASA Quality Publication NPC 200-3, April 1962 entitled, "Inspection System Provisions for Suppliers of Space Materials, Parts Components and Services". Wherever possible, parts shall be selected from the following documents:

1) GSFC-PPL-3, 1 Jan. 65, Preferred Parts List,
2) JPL Preferred Parts List for Spacecraft Scientific Experiments,
3) OGO Electronic Parts Specification Development Guide.

All part ratings shall be derated for design use as necessary to achieve, in conjunction with simplified design and redundance where necessary, the specified reliability for the unit.

The reliability analysis required as a part of the final report shall be based on MIL-HDBK-217, 8 Aug. 62, "Reliability Stress and Failure Rate Data for Electronic Equipment".

All work on this order is subject to inspection and test by NASA or its designated representative at all times (including period of performance) and places. Final acceptance will be performed at GSFC.

4.2 Test Program

The contractor shall fully test each unit to insure full compliance with all electrical and mechanical requirements of the specification.

Although each unit shall be bench-tested as above, only one unit shall be tested for compliance with the environmental requirements, and only the following tests shall be performed (in the order listed):

1) temperature,

2) radio frequency interference,

3) vibration

4) thermal-vacuum

The above tests shall be performed prior to delivery of the units to GSFC.

All measurements shall be made with instruments which have had their accuracy verified periodically against standards traceable to the National Bureau of Standards.

Data shall be provided to GSFC as specified in para. 4.3 of this specification.

4.2.1 Temperature

4.2.1.1 Cold Storage

a) Thermocouples to indicate temperature stabilization shall be attached to the component in sufficient number and at such locations as to measure the highest and lowest component temperature. Stabilization shall be considered achieved when no thermocouple varies by more than $0.5^{\circ}C$/hr.

b) The instrumented component, while non-operative, shall be placed in a test chamber which shall be stabilized at $-30^{\circ}C \pm 2^{\circ}C$. The

component shall ramain so exposed for six hours.

c) Following this exposure, the temperature of the test chamber shall be increased to +25°C ± 5°C and the component operated typical of orbital flight for sufficient duration to determine compliance with its performance specification.

4.2.1.2 Hot Storage

a) The component shall be placed in a nonoperative state and the temperature of the test chamber increased in one hour or less to +70C ± 2°C. After stabilization of chamber temperature, the component shall remain exposed to +70°C for six hours.

b) Following this exposure the temperature of the test chamber shall be reduced to +25° C ± 5°C and the component operated typical of orbital flight. The durationof operation shall be sufficient to determine compliance of the component with its performance.

4.2.1.3 Operational Temperature

a) The instrumented component, while non-operative, shall be placed in a test chamber. The temperature of the chamber shall be adjusted such that the temperature of the component becomes stabilized at -20°C ± 2°C. After temperature stabilization, the component shall be operated for one hour minimum and its performance checked. For cyclically operated components ("on-off" orbital operation), cold start capability shall be demonstrated at least three times. Each cycle of operation shall be

preceded by reverting to stabilized conditions at -20° C ± 2°C. The total duration of operation shall be one hour minimum.

b) Immediately following the cold temperature exposure, the component shall be turned off and the temperature of the test chamber increased to +70°C ± 2°C. After temperature stabilization, the component shall be operated.

c) Following this exposure, the temperature of the test chamber shall be reduced to +25°C ± 5°C and the component operated for sufficient duration to determine compliance with its performance specification.

4.2.2 Vibration

For this test, with the exception of test levels and recording on magnetic tape (recording accelerometer signals shall be recorded continuously; however, the use of magnetic tape is not mandatory) all the requirements of paragraphs 4.1.8 through 4.1.8.5 of specification S-320-D-1 shall apply. Since the tests must be performed in the asbsence of both a representative spacecraft structure and transmissibility measurements, the component shall be attached to the vibration excitor via a rigid fixture. Sinusoidal virbration test levels shall be as specified in paragraph 4.2.2.1. Random virbration test levels shall be as specified in paragraph 4.2.2.2.

4.2.2.1 Sinusoidal Vibration

This test shall be conducted by sweeping the applied frequency once through each range specified in the schedule. The rate of change of frequency shall be 2 octaves per minute.

SINUSOIDAL VIBRATION SCHEDULE

Axis	Frequency Range cps	Test Duration Min.	Acceleration g, 0-to-peak
Thrust (Z-Z)	10-50	1.17	3.8*
	50-110	.57	1.524 mm(.06 inch)** double amplitude constant displacement
	110-200	.43	37.0**
	200-500	.66	7.3
	500-2000	1.00	21.0
	2000-3000	1.00	15.0
	Total	4.83 Min.	

SINUSOIDAL VIBRATION SCHEDULE (con't)

Axis	Frequency Range cps	Test Duration Min.	Acceleration g, 0-to-peak
Lateral (X-X) and Lateral (Y-Y)	10-50	1.17	3.0*
	50-96	.44	.584 mm (.023 inch)** double amplitude constant displacement
	96-250	.72	11.0*
	250-500	.50	2.3
	500-2000	1.00	3.8
	2000-3000	1.00	15.0
	Total	4.83 min. (each axis)	
	Grand Total: 13.49 Minc.		

* When the specified accelerations cannot be attained due to armature displacement limitations, the input may be a constant displacement not less than 0.5 in. double amplitude.

** In these frequency ranges, the test levels include the effects of transmissibilities through the spacecraft structure as explained in paragraph 4.3.4 of S-320-D-1.

4.2.2.2 Random Motion Vibration

Gaussian random vibration shall be applied with the "g-peaks" clipped at three times the root-mean-square acceleration specified in the schedule. With the component installed, the control accelerometer response shall be equalized such that the specified power spectral density (PSD) values are within ± 3 db throughout the frequency band as determined by the analysis specified in 4.1.8.3 of specification S-320-D-1. The filter roll-off characteristic above 200 cps shall be at a rate of 40 db/octave or greater.

RANDOM VIBRATION SCHEDULE

Axis	Frequency Range cps	Test Duration Min.	PSD Level g^2/cps	Acceleration g-rms
Thrust (Z-Z) Lateral (X-X) Lateral (Y-Y)	20-2000	4 (each axis)	0.07	11.8
		Total: 12 Min.		

4.2.3 Thermal-Vacuum

The component shall be mounted in such a manner that it is thermally isolated from its mounting fixture. The mounting fixture for this purpose shall be designed to minimize interference of radiation paths from the radiant sources to the component. The component shall be installed in the chamber in such a way that it will not be exposed to any abnormally hot or cold source. Thermocouples shall be attached to the component in sufficient number and at such locations as to measure the highest and lowest component temperature. The instrumented component shall be placed in the test chamber, and an operational check shall be performed prior to chamber evacuation. With the component operative, typical of boost phase, the chamber shall be evacuated to 10^{-12} TORR. Corona effects shall be monitored throughout the evacuation period.

4.2.3.1 Low-Temperature Soak

Immediately following the corona check, the component shall be turned

off and the chamber adjusted such that stable conditions are established at 10^{-13} torr and $-20^{\circ}C \pm 2^{\circ}$ C. Stabilization shall be assumed when indication from each thermocouple attached to the component does not change by more than $0.5^{\circ}C$ per hour. The chamber control shall be held fixed, and the component operated throughou the exposure period of 24 hours. For cyclically-operated components ("on-off" orbital operation), cole start capability shall be demonstrated at least three times during the 24-hour exposure. Each cycle of operation shall be preceded by reverting to stabilized conditions at $-20^{\circ}C \pm 2^{\circ}C$. The temperature of the component shall be monitored continuously during the exposure. Performance of the component shall be monitored at least at the beginning and end of the exposure period. For cyclically-operated components, the performance of the component shall be checked periodically, consistent with the test duty cycle.

4.2.3.2 High-Temperature Soak

At the conclusion of the low-temperature vacuum exposure, the chamber conditions shall be altered such that stable conditions are re-established at 10^{-13} torr and $+70^{\circ}C \pm 2^{\circ}C$. Stabilization shall be assumed when indication from each thermocouple does not change by more than $0,5^{\circ}C$ per hour. When stable conditions have been achieved, the chamer temperature controls and its temperature held fixed. The component shall be operated and its temperature monitored throughout the exposure period of 24 hours. The performance of the component shall be checked periodically as well as at the beginning and end of the exposure period.

4.2.4 Radio Frequency Interference

Test shall be performed to prove complicane with all requirements of paragraph 3.4.7.

4.3 Documentation

The basic philosoply of the data required hereunder is that it must be sufficient to summarize the program, document technical advances, fully describe developed equipment, and in particular, to permit fabrication, adjustment, test and operation of developed equipment by any qualified source.

4.3.1 Monthly Letter Reports

Informal monthly letter reports shall be provided in 3 copies by the 10th of the month following the report (calander) month. They shall comply with requirements of TID-S-100 for type I reports, and shall include:

(1) summary of work performed during the month;

(2) special problems and their solutions;

(3) whether project on schedule and whether funding adequate to complete the program;

(4) work plan for the coming month;

(5) recommendations, if any, for desirable specification changes;

(6) a reliability analysis;

(7) a complete failure analysis;

(8) radiation effects analysis;

(9) complete design information and drawings for any test jigs used in testing the unit;

(10) test procedures.

5. Preparation for Delivery

5.1 General

Equipment prepared for delivery shall be packaged in manner to ensure delivery without damage. It shall be enclosed by a vapor barrier, which shall contain a desiccant. The humidity state shall be ascertainable without breakage of the vapor seal. The packaging shall also be suitable for storage. The package and equipment shall survive a temperature range (non-operating) of $-30^{\circ}C$ to $+70^{\circ}C$.

5.2 Shipping Instructions

The F. O. B. destination shall be Goddard Space Flight Center, Greenbelt, Maryland. Packages shall be marked as follows:

National Aeronautics and Space Administration

Goddard Space Flight Center

Code 615

Greenbelt, Maryland 20771

Attention: Dr. R. G. Stone

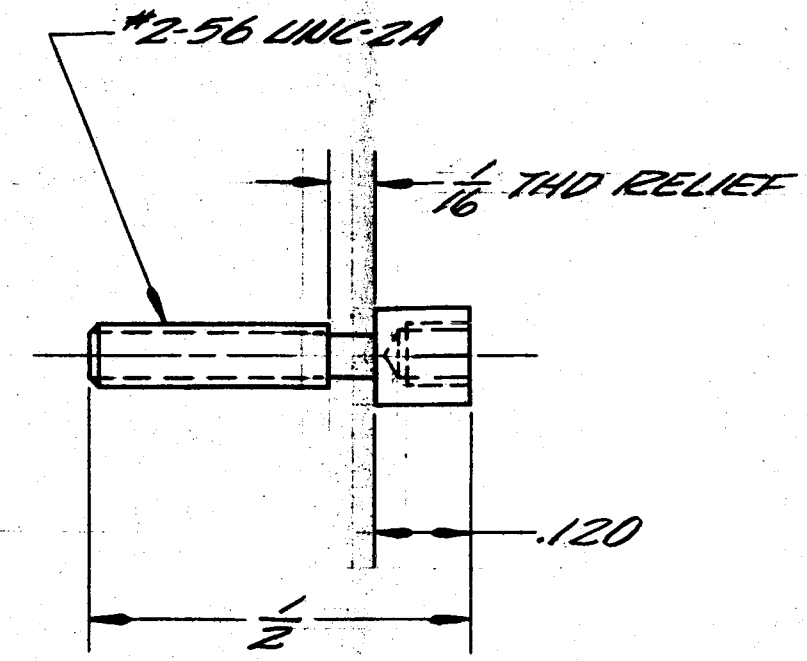
HANDLE WITH EXTREME CAUTION

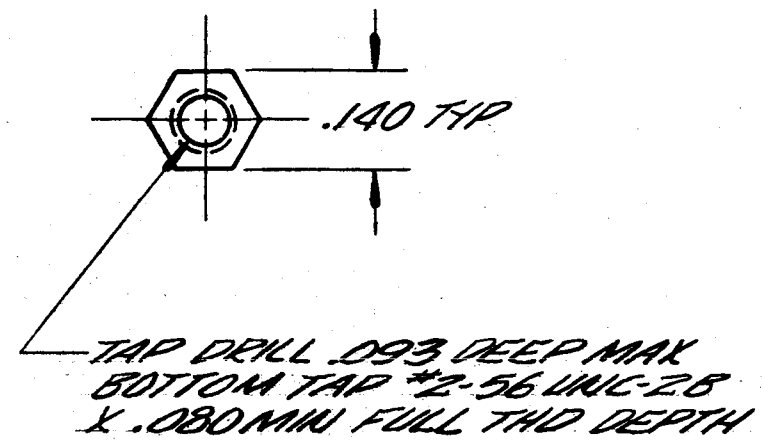
Completed hardware shall be packaged as specified by level C of FED- STD-102.

REV	DATE	BY	DESCRIPTION	APPVD

NOTES: UNLESS OTHERWISE SPECIFIED:

1. 63√ FINISH ALL OVER





WTA - 2158-B-483

	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

LIST OF MATERIAL

2158-F-486	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL CRES 303

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± 1/64
DECIMALS ± .005, ANGLES ± —

SCALE: 4/1
FINISH: NOTED
CLIENT:

NAME	INIT	DATE
DESIGNER		
DRAWN WTA		
CHECKED		
APPROVED		
APPROVED		

RAE

STANDOFF

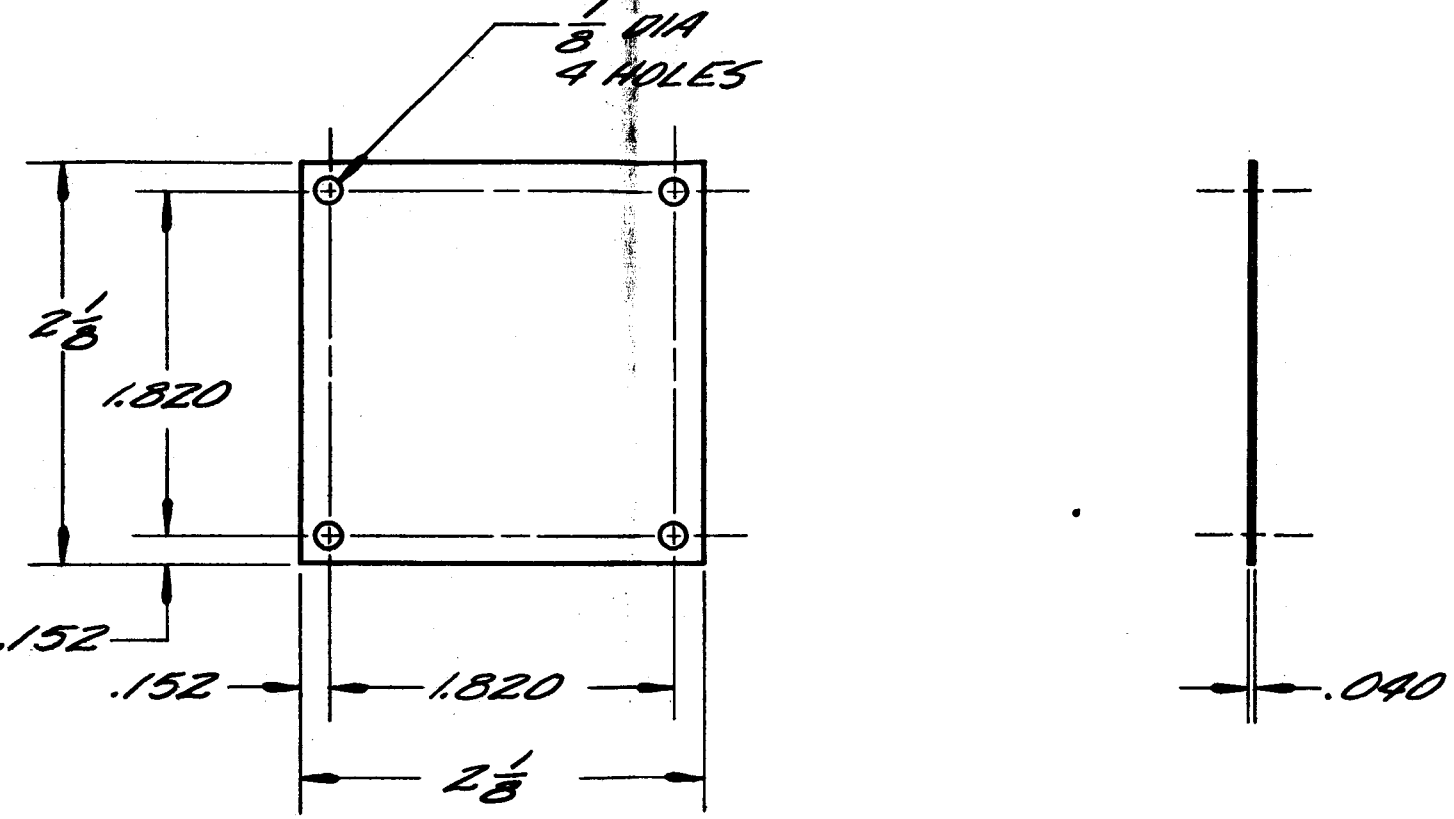
SCALE	UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GB-RAE-1155-001

CODE	SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD



W.T.A. 2158-B-485

LIST OF MATERIAL

2158-F-486	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL TEFLON

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± 1/64
DECIMALS ± .005 ANGLES ± —

SCALE: 1/1
FINISH:
CLIENT:

NAME	INIT	DATE
DESIGNER		
DRAWN WTA		
CHECKED		
APPROVED		
APPROVED		

RAE

BOARD, INSULATOR

SCALE | UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GB-RAE-1155-002

CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD

NOTES: UNLESS OTHERWISE SPECIFIED:

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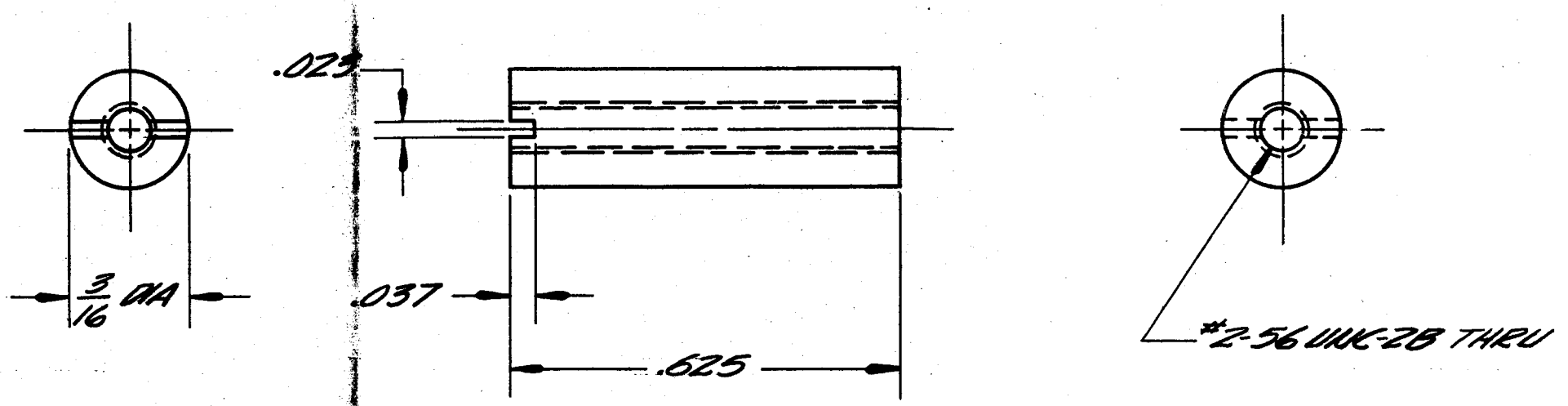

W.T.A. 2158-B-484

2158-F-486	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL BRASS

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± 1/64
DECIMALS ±.005, ANGLES ± ——

SCALE: 4/1

FINISH: NOTED

CLIENT:

LIST OF MATERIAL

NAME	INIT	DATE
DESIGNER		
DRAWN WTA		
CHECKED		
APPROVED		
APPROVED		

RAE

SPACER

SCALE | UNIT WT

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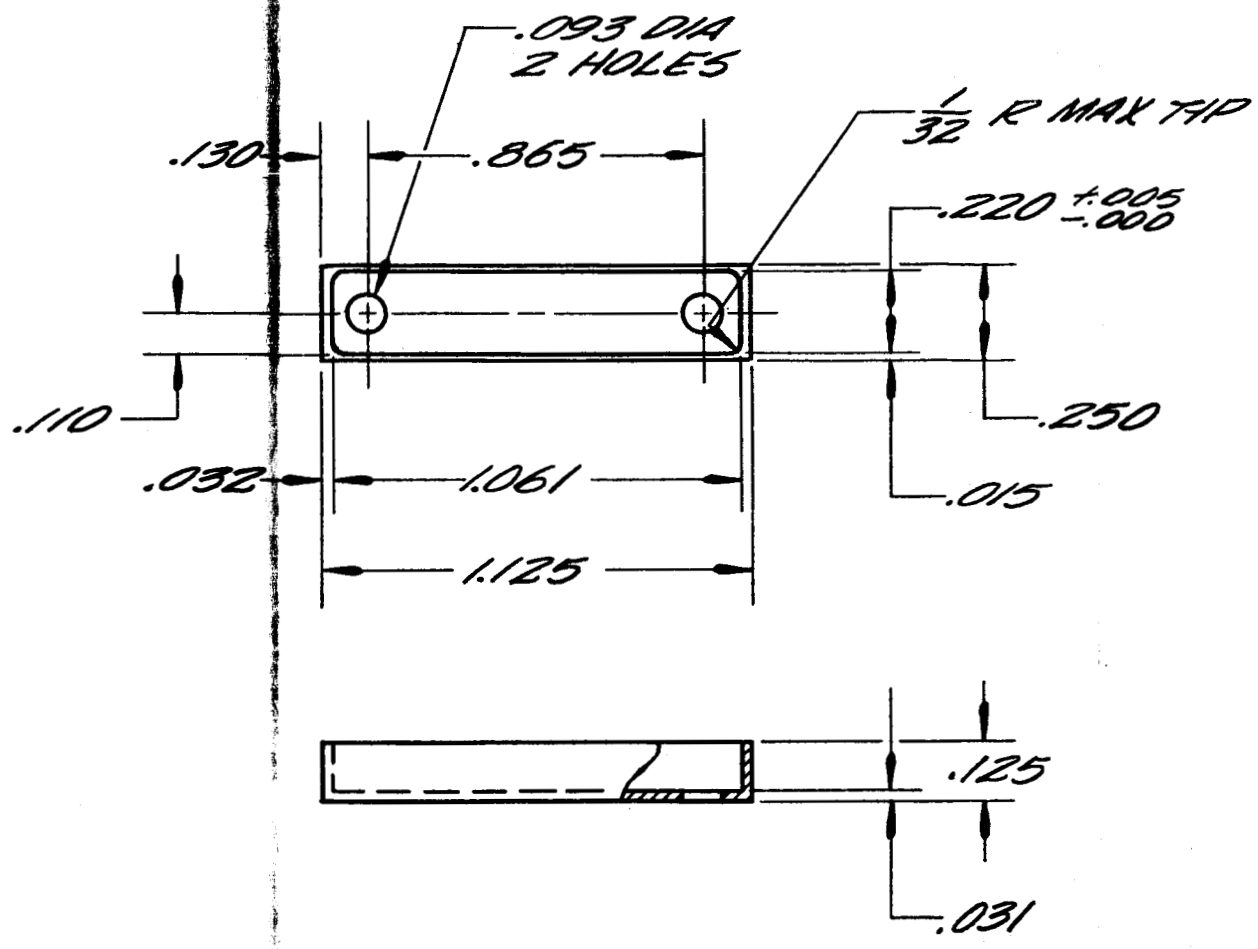
GB-RAE-1155-003

CODE | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED:

1. $\sqrt{63}$ FINISH ALL OVER
2. FINISH: IRIDITE #15A MIL
   ALLIED RESEARCH
   BALTIMORE, MARYLAND

REV	DATE	BY	DESCRIPTION	APPVD



WTA - 2158-B-481

LIST OF MATERIAL

2158-F-486	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL MAGNESIUM AZ31B

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ±1/64
DECIMALS ±.005, ANGLES ±—

SCALE: 2/1
FINISH: NOTED
CLIENT:

NAME	INIT	DATE
DESIGNER		
DRAWN WTA		
CHECKED		
APPROVED		
APPROVED		

RAE
CAN

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GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GB-RAE-1155-004

CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD

A. Encapsulation Procedure

1. Trim all modules to dimensions shown on individual welded module drawings.

2. Load Header, (top A layer film with module output lead locations triangles - punched), leaving headers at least 1/4 inch larger on all sides than the welded module.

3. Q. C. for proper loading and header punching.

4. Insert welded module leads through a 1/16" thick strip of RTV-11, or equivalent, using a strip of styrafoam for backing (See Figure 1).

5. Preheat welded modules in a 70° - 80°C oven for at least 15 minutes.

6. Conformal coat welded modules with sufficient epoxy (Armstrong C-7--see Preparation of Epoxy) to bridge all components and to run between all layers of film. (Note: The amount of epoxy to be used is proportional to the component density of the module.) The epoxy should be applied with Walsco Electronics No. 987 Chem-O-Jector, or equivalent. It should be noted that the epoxy should be applied as quickly as possible since the modules cool rapidly upon exposure to room temperature.

7. Return modules to oven and heat at 70° - 80°C for 15 minutes (Caution: Make sure modules are in a horizontal position as shown in Figure 2. This will allow excess epoxy to run off modules.)
Then turn over the module holding device, such that the module top in Figure 2 is now in the bottom position. (Note: At this point any excess epoxy may be wiped from the surface of the modules with a small mixing splint). Leave the modules in the oven for an additional 15 minutes.

8. Remove the modules from the oven and let cool at room temperature for 4 or more hours before removing the modules from the RTV-11 strip and styrafoam backing material. After removal from the RTV-11 strip, trim the headers to size as indicated on the individual welded module drawings.

B. Preparation of Epoxy

1. Materials

   a. Armstrong Epoxy Resin Products (C-7) resin

   b. Armstrong Epoxy Resin Products activator (W)

2. Mixture

   a. C-7 - - - - - - - - - - - - - - - - - 35 grams

   b. Activator W - - - - - - - - - - - - -15 grams

   (i.e., 7 to 3 parts by weight (Pbw) Resin to Activator respectively to allow for minimum outgassing requirements of the epoxy).

3. Mix the resin and activator thoroughly for at least 5 minutes, then set aside for 15 minutes at room temperature to allow the trapped air bubbles to rise to the surface. Stir lightly at 5 minute Intervals. Then fill the syringe. The epoxy is now ready for Step (6) of Encapsulation Procedure.

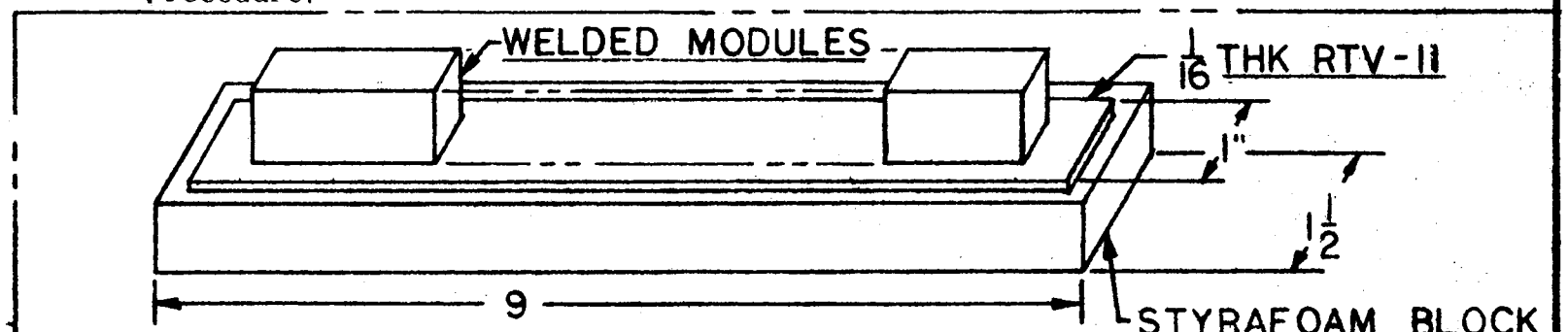


FIG 1

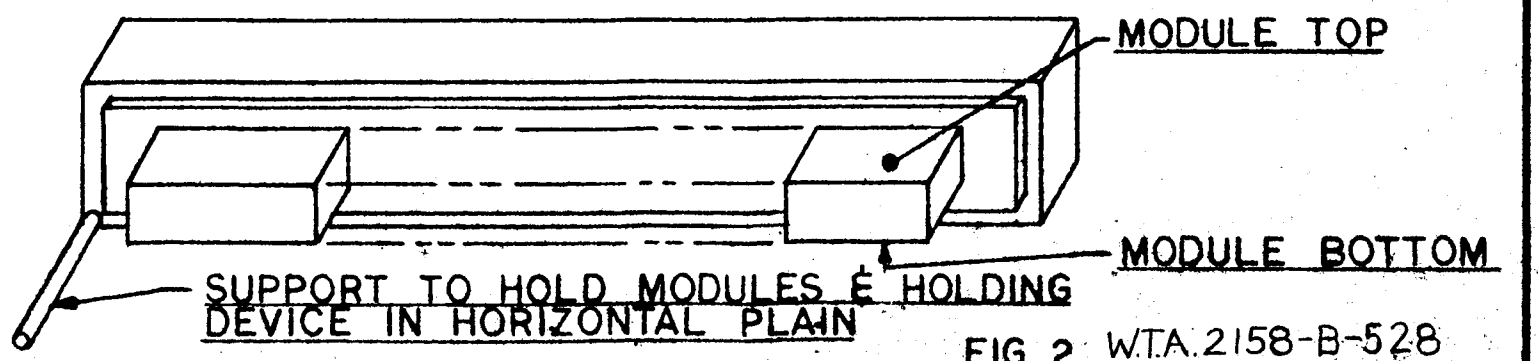


FIG 2 W.T.A.2158-B-528

NEXT ASSY.	USED ON	MATERIAL ———		
APPLICATION		DO NOT SCALE THIS DRAWING		
		REMOVE BURRS, BREAK SHARP EDGES		
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS ± ~ DECIMALS ± ~ , ANGLES ± ~	SCALE: ~ FINISH: ~ CLIENT: NRL	

NAME	INIT	DATE
DESIGNER		
DRAWN WTA		
CHECKED		
APPROVED		
APPROVED		

RAE
ENCAPSULATION PROCEDURE

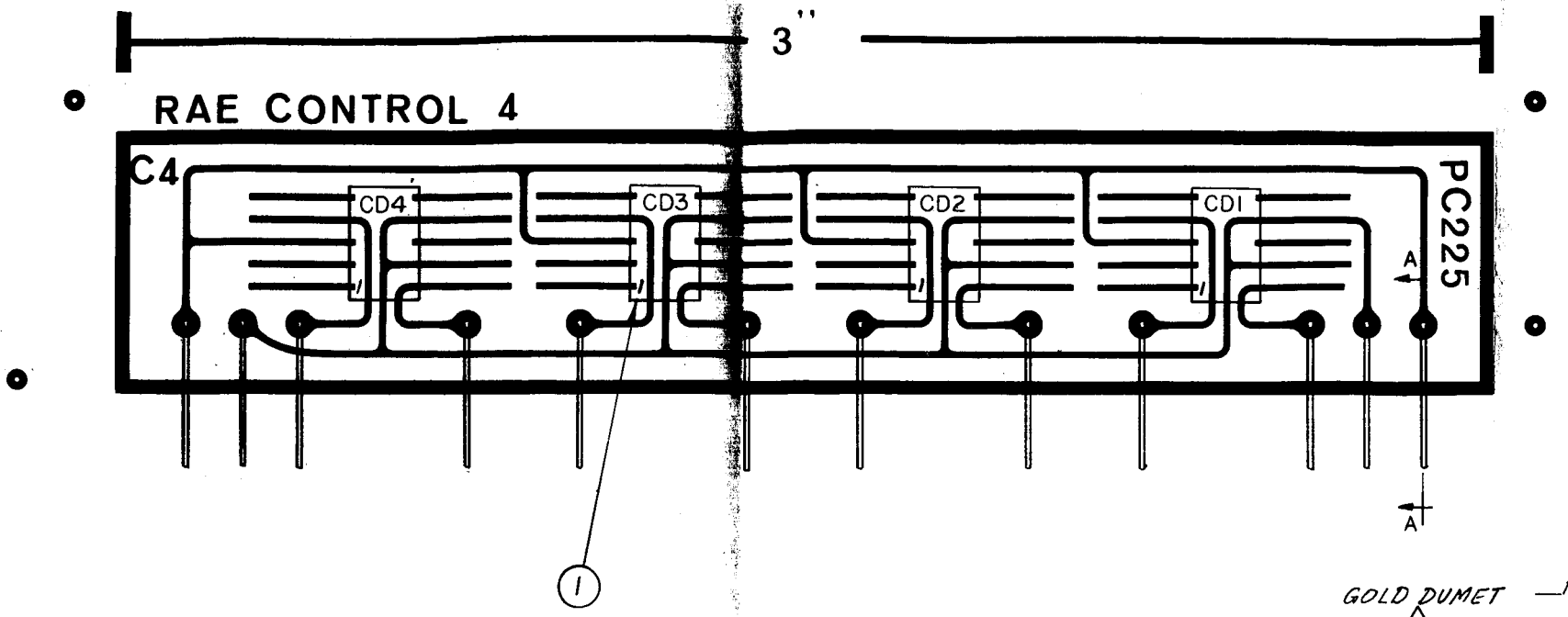
SCALE | UNIT WT

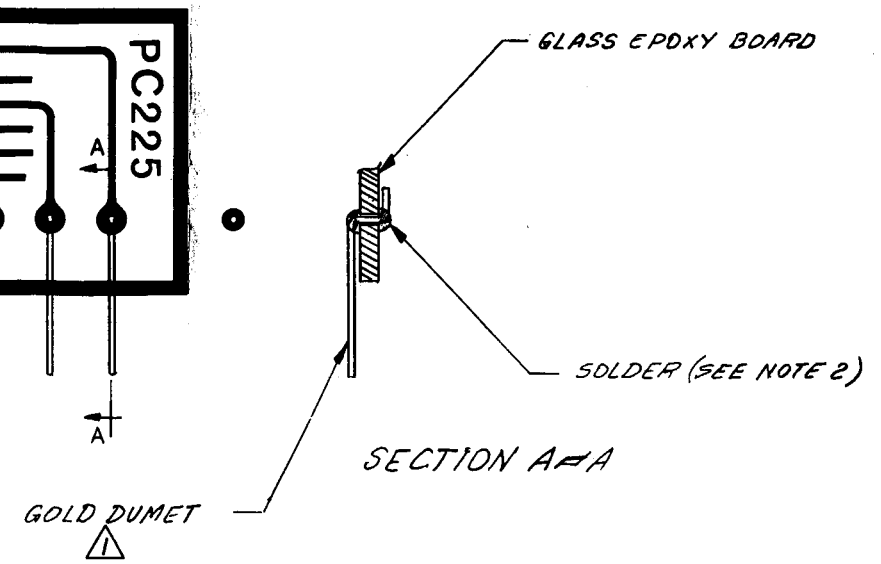
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

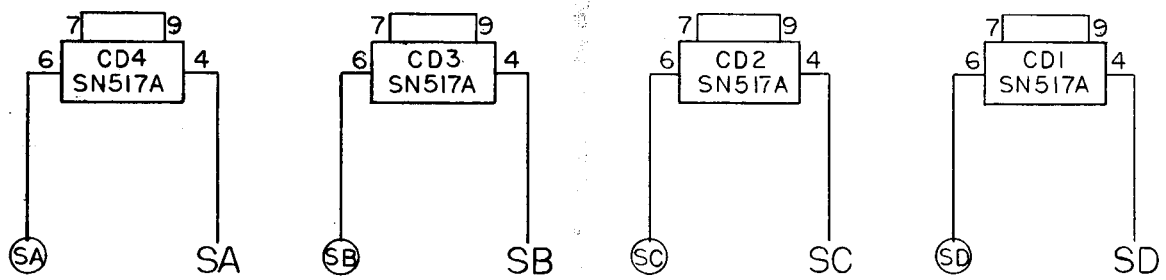
GB-RAE-1155-005

CODE | SHEET OF

REV	DATE	BY	DESCRIPTION	APPVD







CIRCUIT COMPONENT LIST			
FIND NO.	NO. REQD	DESCRIPTION	REMARKS
1	4	SN517A CLOCK DRIVER	T.1

NOTES:
1. PRIOR TO COMPONENTS, INSTALL OUTPUT LEADS .020 GOLD DUMET.
2. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

WTA 2158-C-497

		MATERIAL	NAME	INIT	DATE
			DESIGNER		
			DRAWN	WTA	
		DO NOT SCALE THIS DRAWING	CHECKED		
		REMOVE BURRS, BREAK SHARP EDGES	APPROVED		
2158-R-501		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS DECIMALS ANGLES	SCALE: 4/1		
NEXT ASSY.	USED ON		FINISH:		
APPLICATION			CLIENT:	APPROVED	

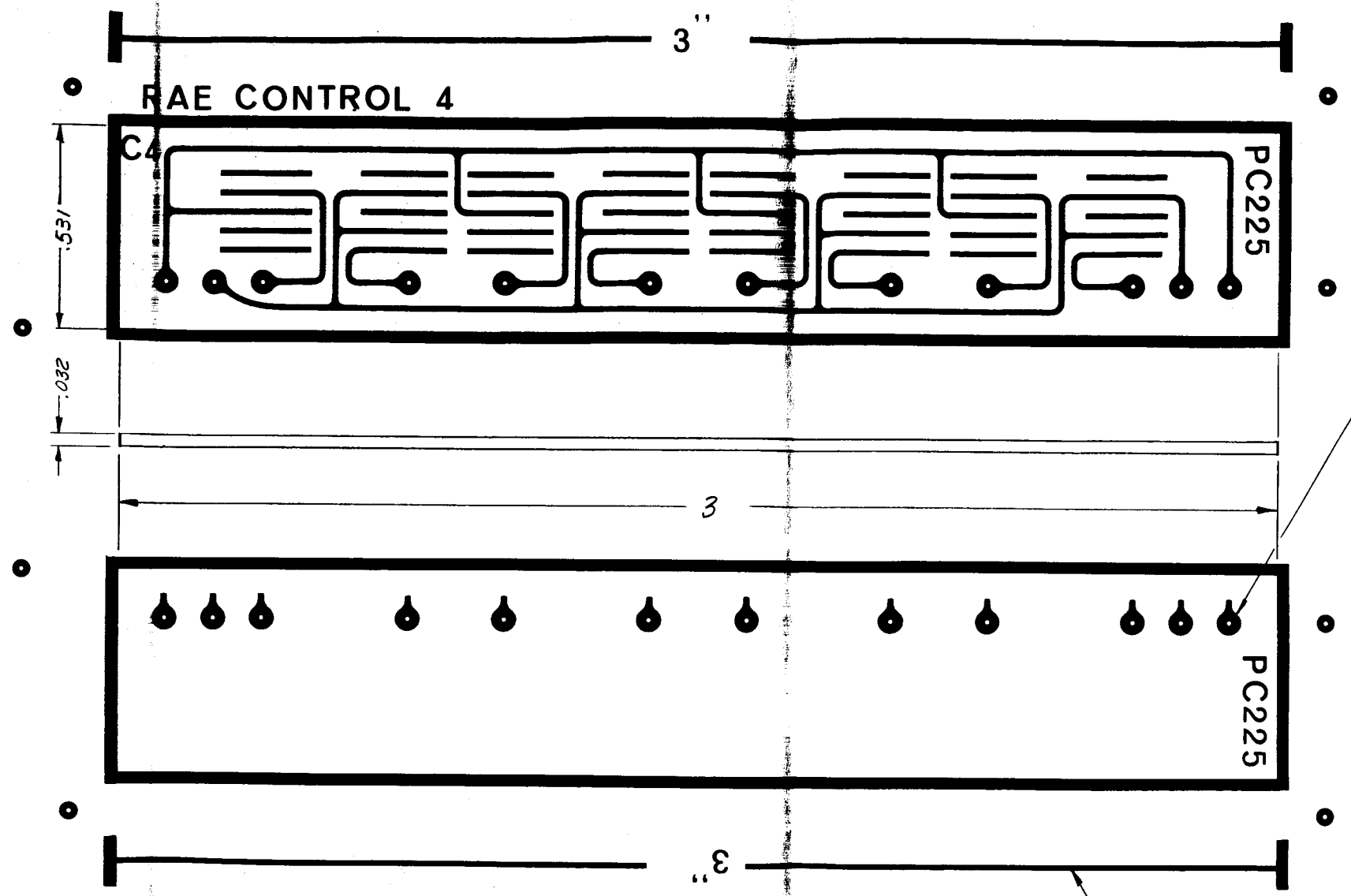
RAE
PRINTED WIRING ASSY.
CONTROL # 4

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GC-RAE-1155-006

SCALE	UNIT WT	CODE	SHEET OF

REV	DATE	BY	DESCRIPTION	APPVD



.025 #71 DRILL
12 HOLES

REF. DIMENSION FOR REDUCTION

NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE .032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT STANDARD MSFC-STD-154.

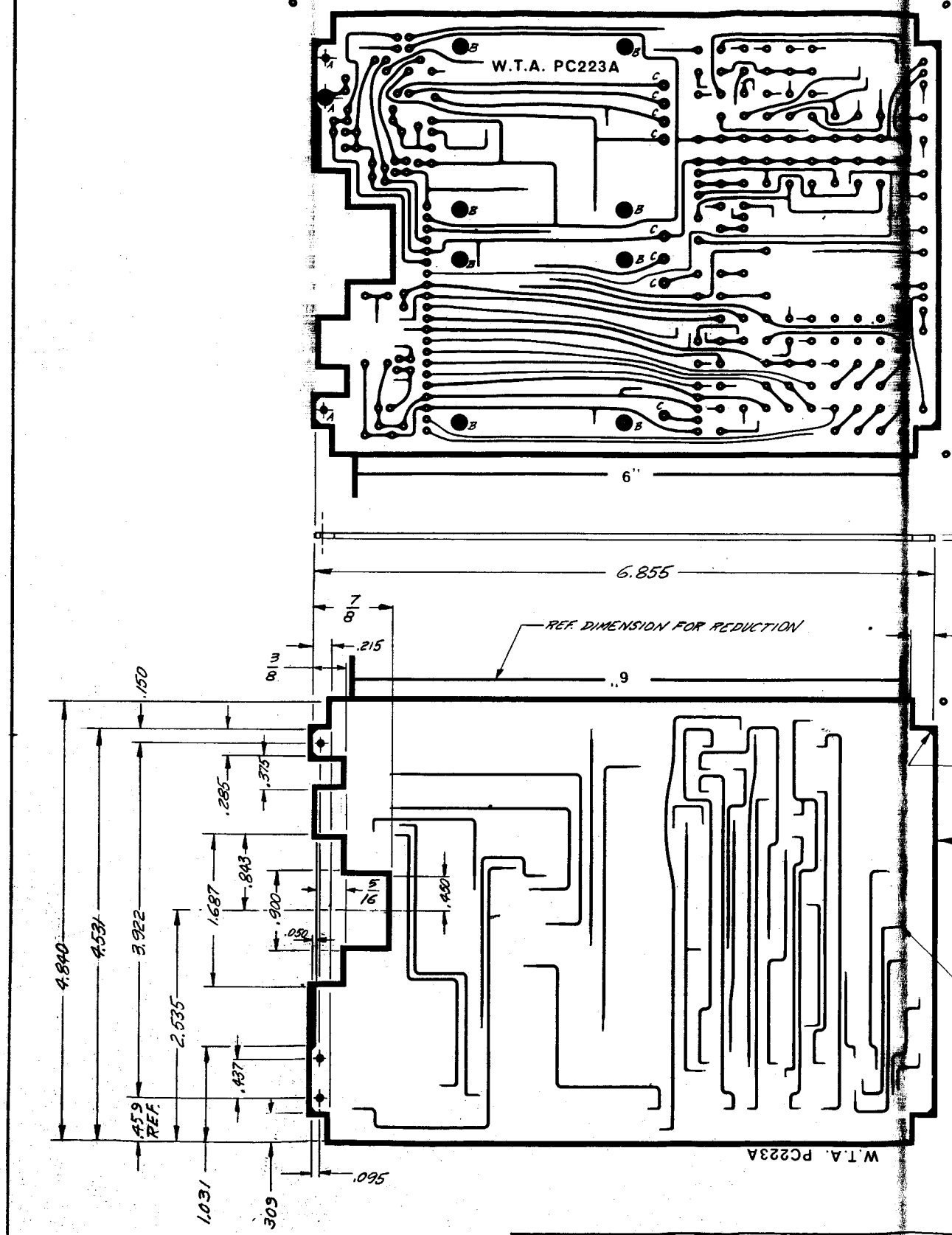
WTA 2158-C-498

		MATERIAL SEE NOTE 1	NAME	INIT	DATE	RAE PRINTED WIRING BOARD CONTROL #4
			DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		DO NOT SCALE THIS DRAWING	DRAWN	W.T.A.		
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED			GC-RAE-1154-007
2158-C-497		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES SCALE: 4:1	APPROVED			
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS FINISH:	APPROVED			
APPLICATION		DECIMALS .XX .XXX . ANGLES CLIENT:	SCALE	UNIT WT	CODE	SHEET OF

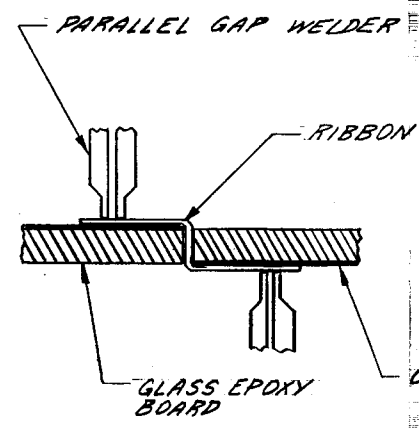
REV	DATE	BY	DESCRIPTION	APPVD

NOTES:

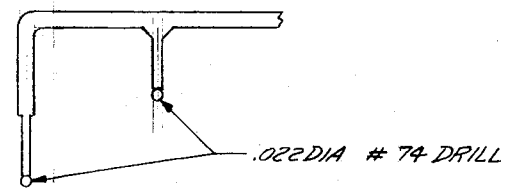
1. GLASS EPOXY LAMINATE SHEET. 2 OZ. COPPER CLAD, GOLD PLATED. FL GE .062 C2.
2. FABRICATE P.C. BOARDS IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.



HOLE DATA		
SYM	QTY	HOLE SIZE
A	3	# 38 DRILL
B	8	# 42 DRILL
C	8	# 55 DRILL
ALL OTHERS		# 70 DRILL



DETAIL B
SCALE 4:1



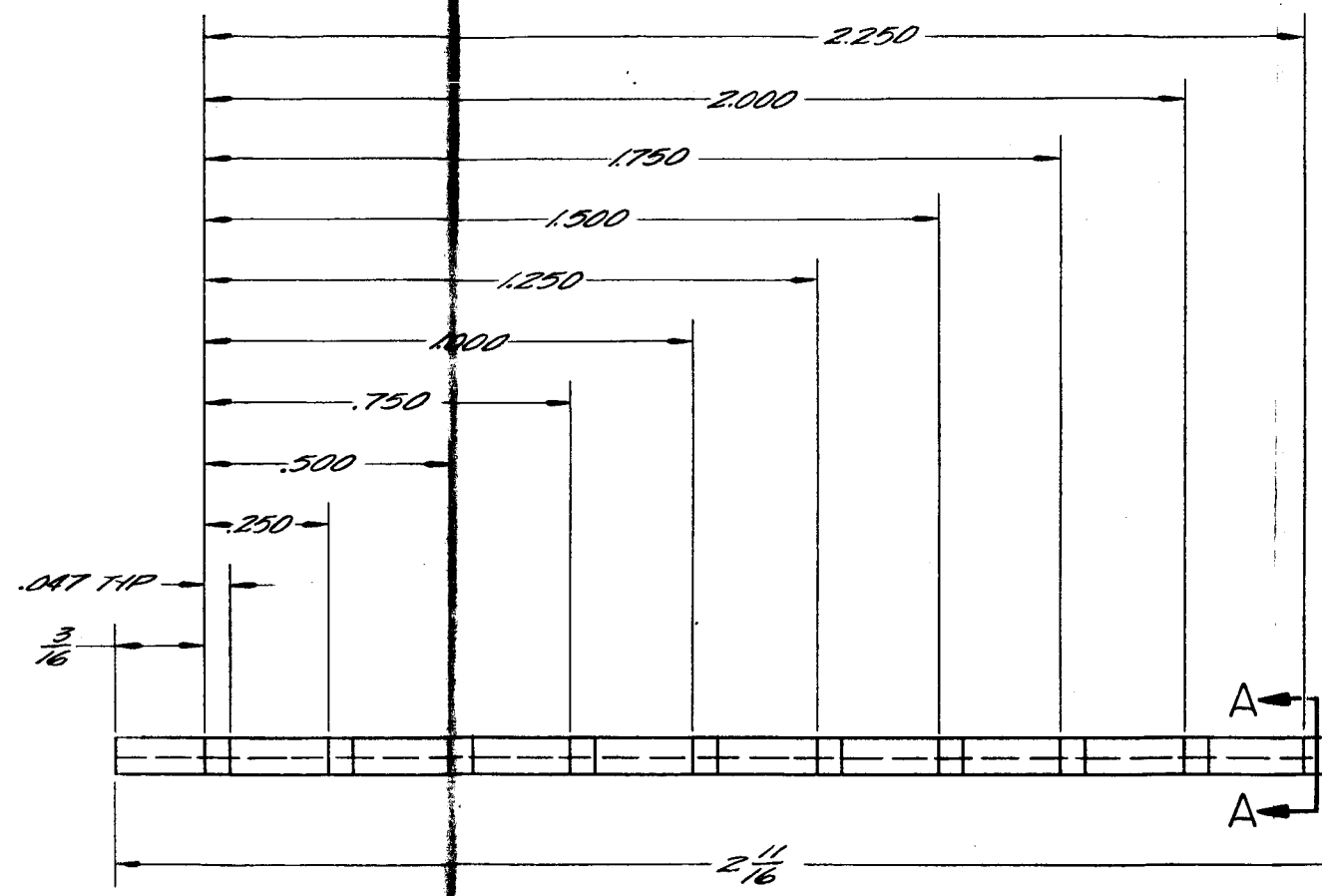
DETAIL A
SCALE 4:1

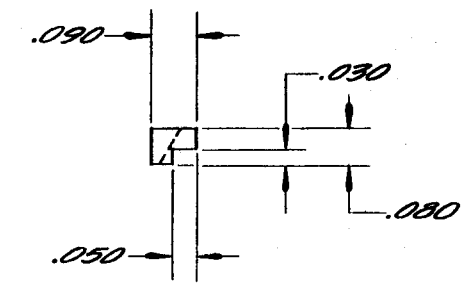
WTA 2158-C-502

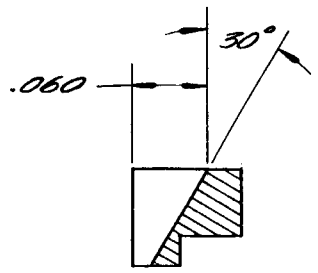
MATERIAL GLASS EPOXY G-10 SEE NOTE 1.		NAME	INIT	DATE	RAE PRINTED WIRING BOARD, MAIN
DO NOT SCALE THIS DRAWING		DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
REMOVE BURRS, BREAK SHARP EDGES		DRAWN	WTA		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 1:1	CHECKED			GC-RAE-1155-008
TOLERANCE ON FRACTIONS ± 1/64	FINISH:	APPROVED			
DECIMALS ± .005, ANGLES ±	CLIENT:	APPROVED			
2158-R-501 NEXT ASSY. USED ON APPLICATION					SCALE UNIT WT CODE SHEET OF

DIETZGEN NO. 168M AGEPROOF VELLUM 1161

REV	DATE	BY	DESCRIPTION	APPVD





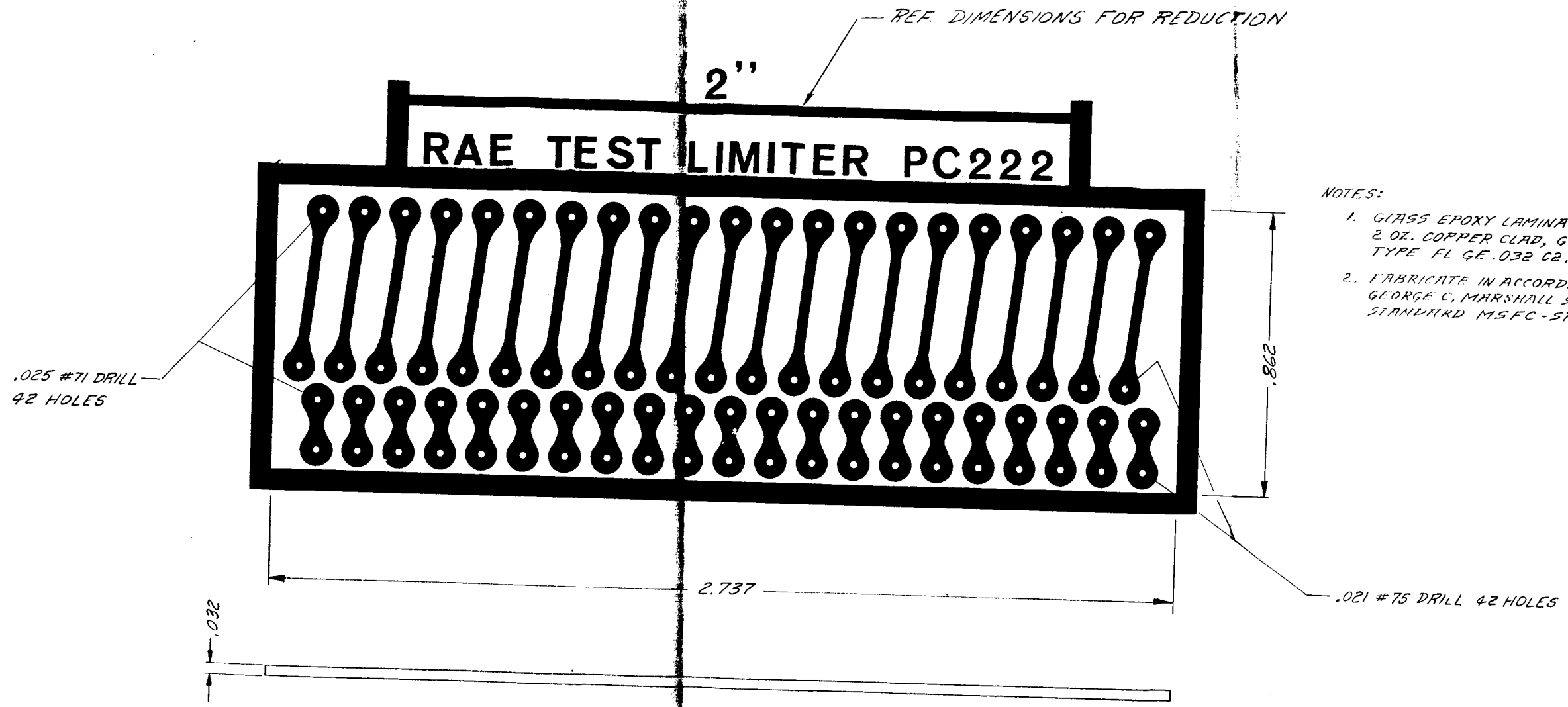


SECTION A-A
SCALE: 10/1
TYP 10 PLACES

WTA 2158-C-482

		MATERIAL NYLON	NAME	INIT	DATE	RAE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
			DESIGNER			RETAINING STRIP	
		DO NOT SCALE THIS DRAWING	DRAWN	WTA			
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED				GC-RAE-1155-009
2158-F-486		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS ± 1/64 DECIMALS ± .005, ANGLES ± 2°	SCALE: 3/8 HALF	APPROVED		SCALE	UNIT WT
NEXT ASSY.	USED ON		FINISH:			CODE	SHEET OF
APPLICATION			CLIENT:	APPROVED			

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED. TYPE FL GE .032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT STANDARD MSFC-STD-154.

WTA 2158-C-496

2158-D-495	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL SEE NOTE 1

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ±
DECIMALS ±.005. ANGLES ±

SCALE: 4:1
FINISH:
CLIENT:

	NAME	INIT	DATE
DESIGNER			
DRAWN	WTA		
CHECKED			
APPROVED			
APPROVED			

RAE
PRINTED WIRING BOARD
TEST LIMITER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

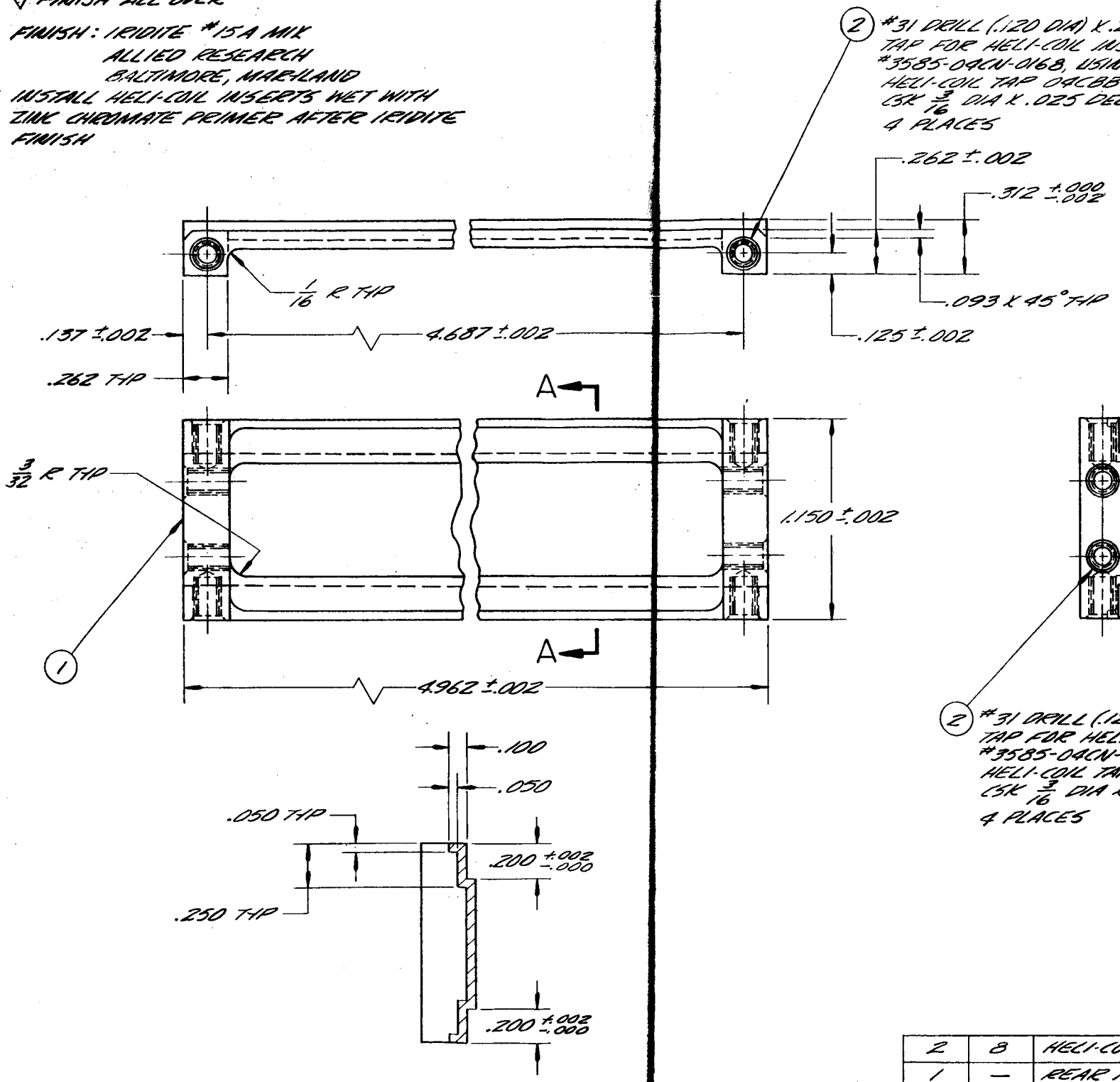
GC-RAE-1155-010

SCALE | UNIT WT | CODE | SHEET OF

REV	DATE	BY	DESCRIPTION	APPVD

NOTES: UNLESS OTHERWISE SPECIFIED:

1. 63 FINISH ALL OVER
2. FINISH: IRIDITE #15A MIX
   ALLIED RESEARCH
   BALTIMORE, MARYLAND
3. INSTALL HELI-COIL INSERTS WET WITH ZINC CHROMATE PRIMER AFTER IRIDITE FINISH



SECTION A-A

WTA 2158-C-477

ITEM NO.	NO. REQD	NOMENCLATURE	MATERIAL	REMARKS
2	8	HELI-COIL INSERT	#3585-04CN-0168	NON-MAGNETIC HELICOIL CORPORATION DANBURY, CONN.
1	—	REAR PANEL	MAGNESIUM, AZ31B	5" X 1 7/16 X 3/16 THK

LIST OF MATERIAL

2158-F-486	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL SEE LIST OF MATERIAL

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ± 1/64
DECIMALS ± .005, ANGLES ± 2°

SCALE: 2/1
FINISH: NOTED
CLIENT:

	NAME	INIT	DATE
DESIGNER			
DRAWN	WTA.		
CHECKED			
APPROVED			
APPROVED			

RAE

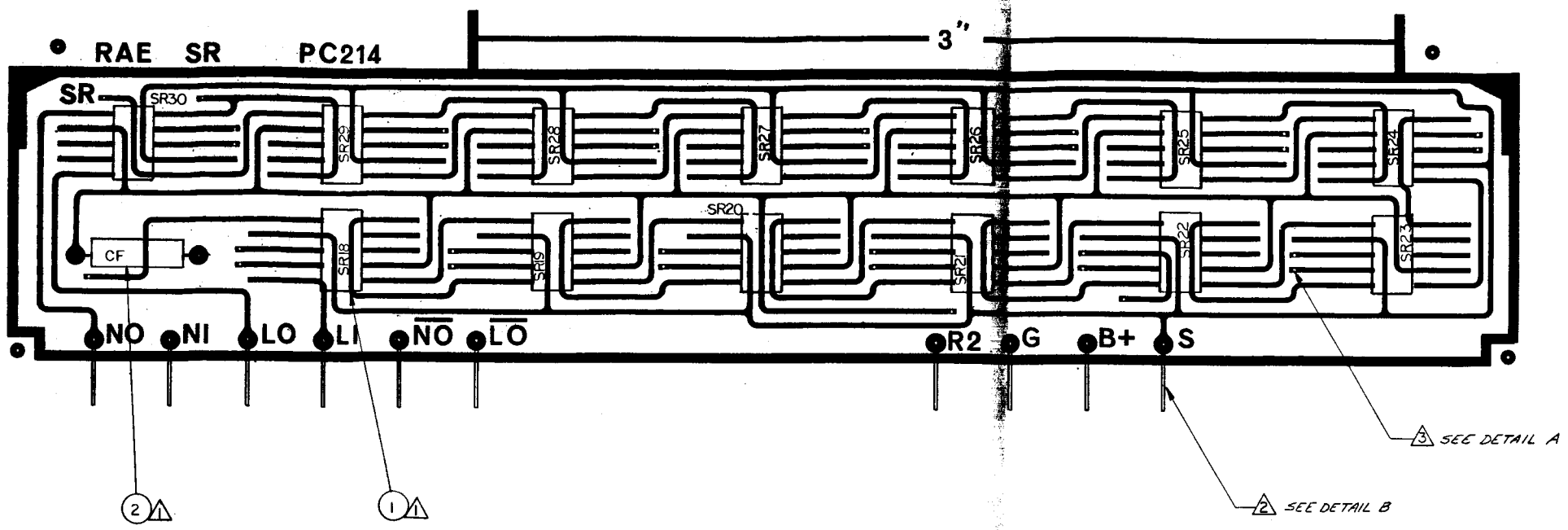
PANEL, REAR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GC-RAE-1155-011

SCALE	UNIT WT	CODE	SHEET OF

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:
1. COMPONENT DESIGNATION SHOWN FOR -1 ASSY ONLY.
2. STEP 1. INSTALL OUTPUT LEADS .020 GOLD DUMET
3. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS, 31 PLACES. FEEDTHRU MATERIAL 0.01 x 0.004 RODAR RIBBON.
4. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

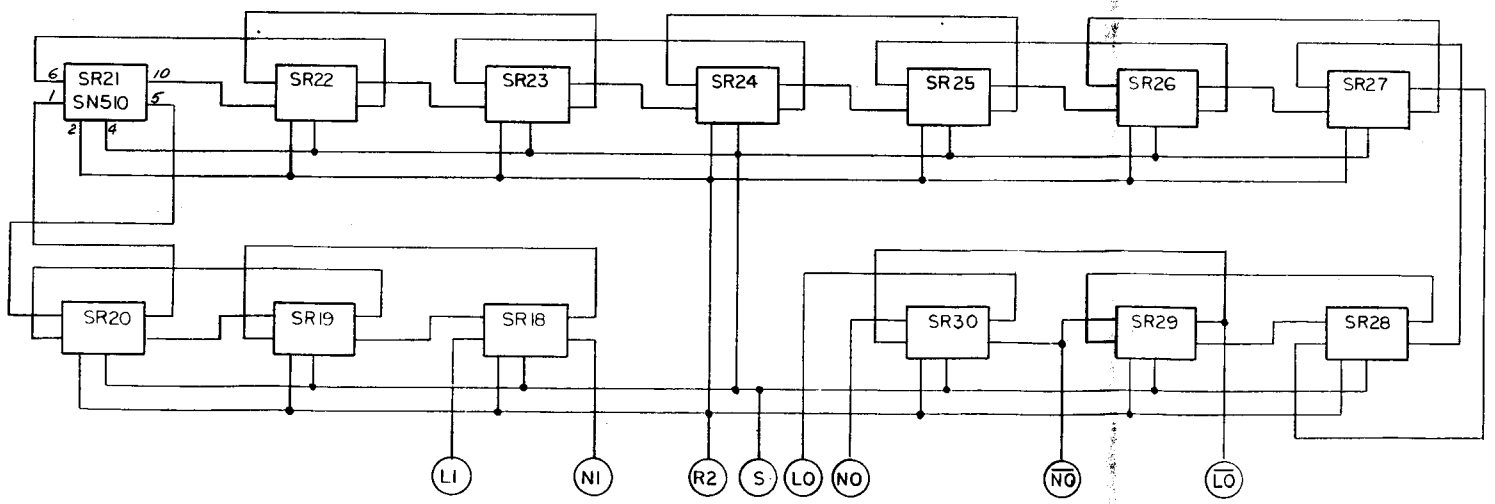
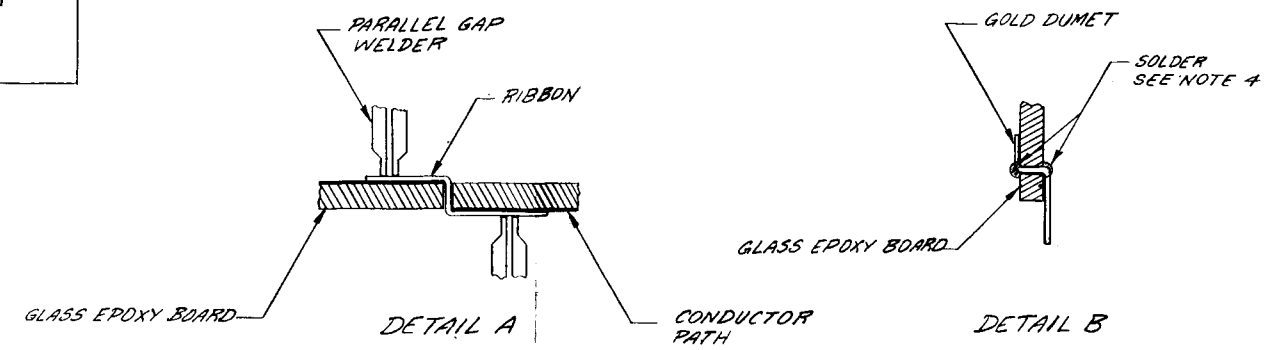


TABLE OF ASSEMBLIES				
FIND NO.	REF. DESIGNATIONS -1	-2	-3	-4
1	SR18 THRU SR30	SR31 THRU SR43	SR44 THRU SR56	SR57 THRU SR68
2	CF	CF	CF	CF

CIRCUIT COMPONENT LIST.			
FIND NO.	NO. REQ'D	DESCRIPTION	REMARKS
1	13	SN510 R-S FLIP-FLOP COUNTER	T.I.
2	1	CAPACITOR 1MFD 350D 15V	SPRAGUE



WTA 2158-D-491

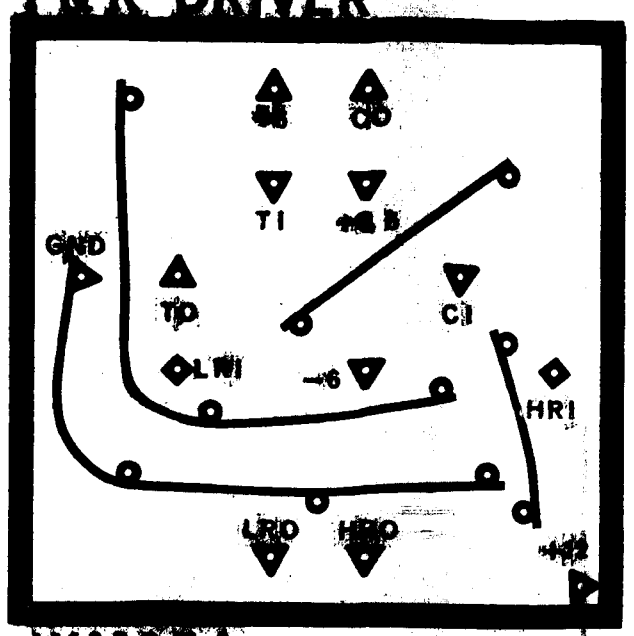
MATERIAL		NAME	INIT	DATE	RAE PRINTED WIRING ASSY SHIFT REGISTER
		DESIGNER			
DO NOT SCALE THIS DRAWING		DRAWN WTA			
REMOVE BURRS, BREAK SHARP EDGES		CHECKED			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1	APPROVED			
TOLERANCE ON FRACTIONS ±	FINISH:	APPROVED			
DECIMALS ± , ANGLES ±	CLIENT:				
2158-R-501 NEXT ASSY. / USED ON APPLICATION					SCALE / UNIT WT / CODE / SHEET 1 OF 1

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

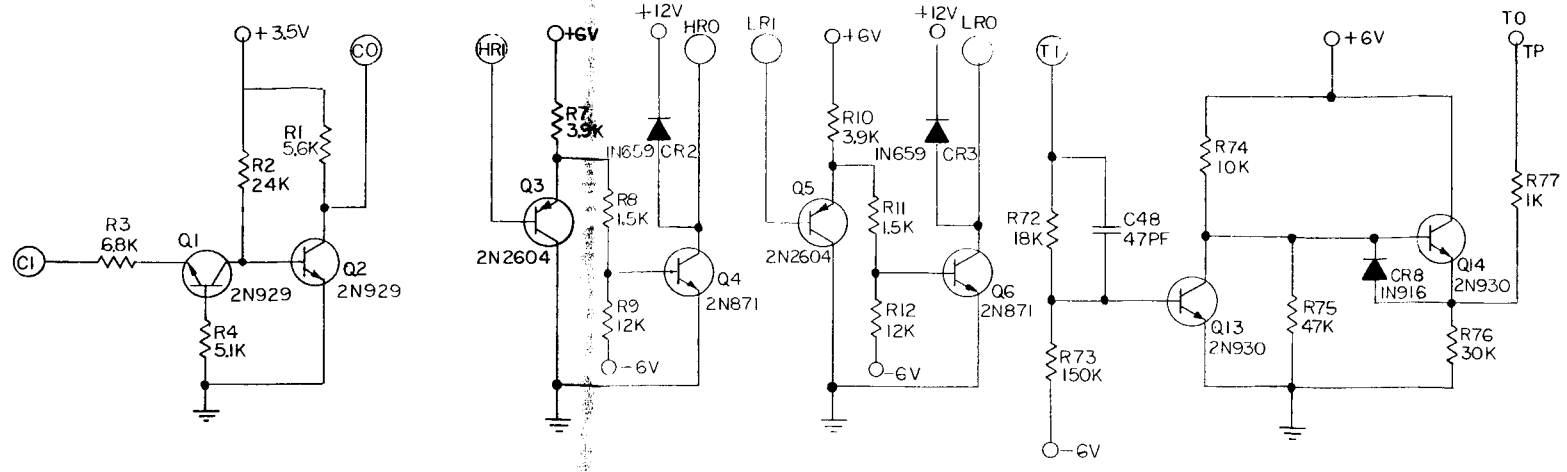
GR-RAE-1155-101

REV	DATE	BY	DESCRIPTION	APPVD

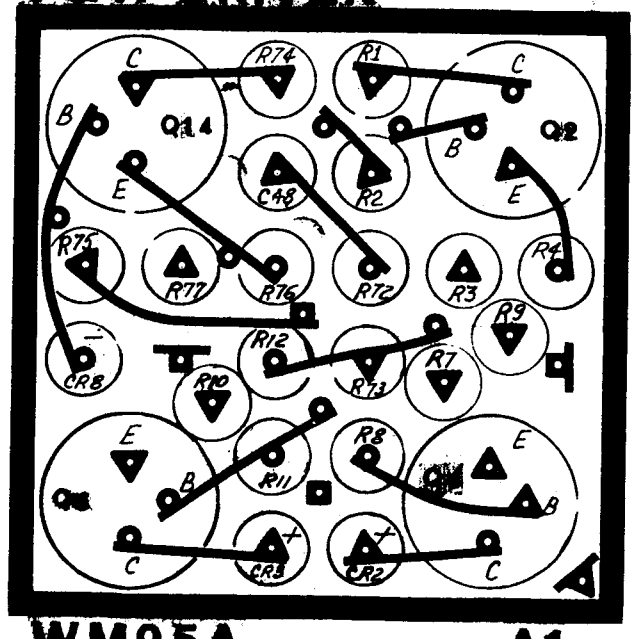
T&R DRIVER



WM95A A2

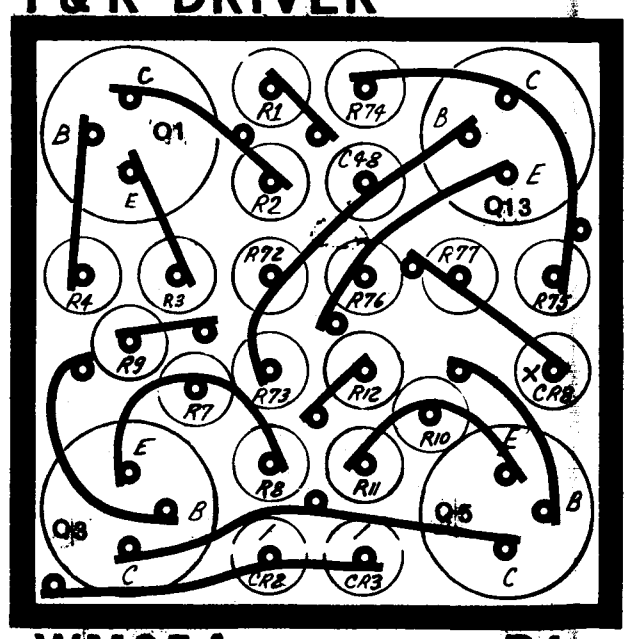


T&R DRIVER

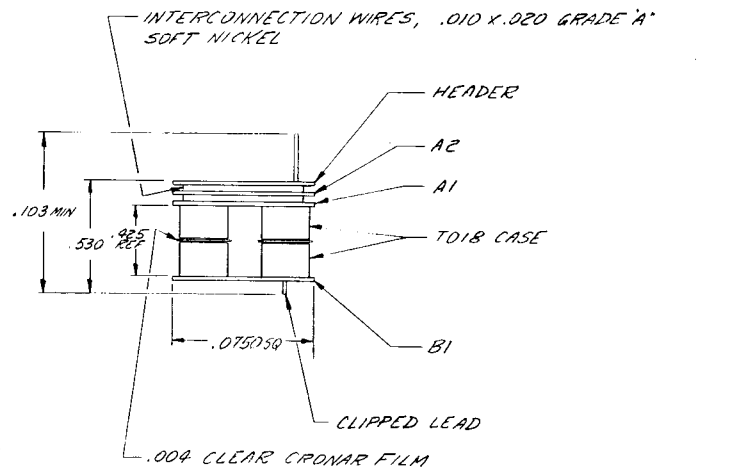


WM95A A1

T&R DRIVER



WM95A B1



UNENCAPSULATED MODULE CONFIGURATION
SCALE: NONE
FOR ENCAPSULATION PROCEDURE SEE DWG NO. 2158-B-528

DESIGN.	DESCRIPTION	REMARKS
Q14	TRANSISTOR 2N930	T.I
Q13	2N930	T.I
Q6	2N871	FAIRCHILD
Q5	2N2604	T.I
Q4	2N871	FAIRCHILD
Q3	2N2604	T.I
Q2	2N929	T.I
Q1	TRANSISTOR 2N929	T.I
CR8	DIODE IN916A	T.I
CR3	DIODE IN916A	T.I.
CR2	DIODE IN916A	T.I.
C48	CAPACITOR 47PF MCBO	AERovox
R77	RESISTOR, 1K 1/4W ± 5%	WELWYN
R76	30K	
R75	47K	
R74	10K	
R73	150K	
R72	18K	
R12	12K	
R11	1.5K	
R10	3.9K	
R9	12K	
R8	1.5K	
R7	3.9K	
R4	5.1K	
R3	6.8K	
R2	24K	
R1	RESISTOR, 5.6K 1/4W ± 5%	WELWYN

LIST OF MATERIAL WTA 2158-D-527

		MATERIAL	NAME	INIT	DATE
			DESIGNER		
		DO NOT SCALE THIS DRAWING	DRAWN WTA		
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED		
2158-R-501		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES SCALE: 8:1	APPROVED		
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± FINISH:	APPROVED		
APPLICATION		DECIMALS ± , ANGLES ± CLIENT:			

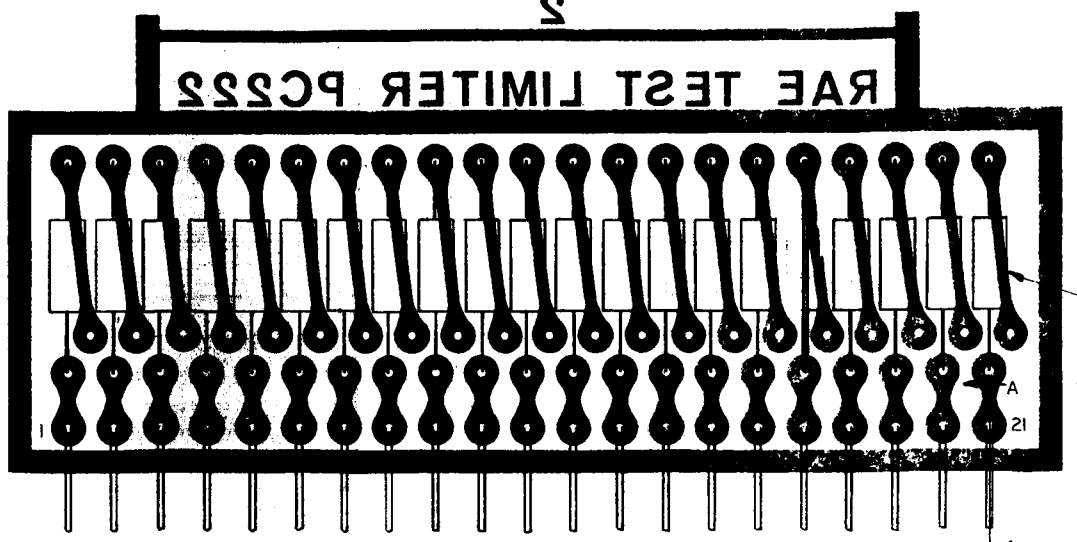
RAE
WELDED MODULE
T&R DRIVER

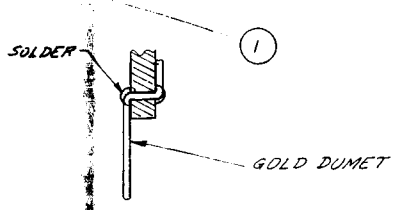
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-1155-203

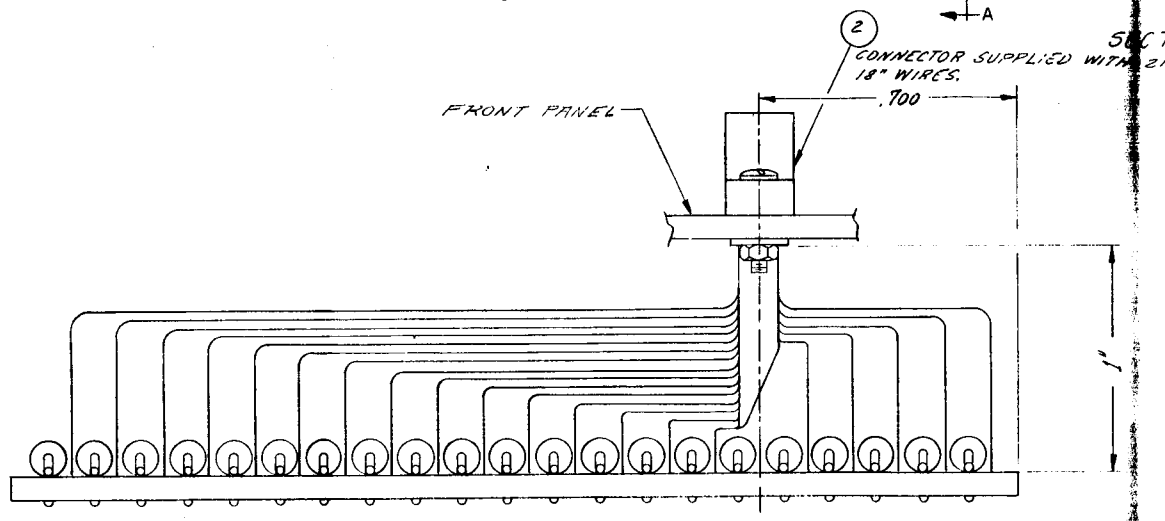
SCALE | UNIT WT | CODE | SHEET 1 OF 1

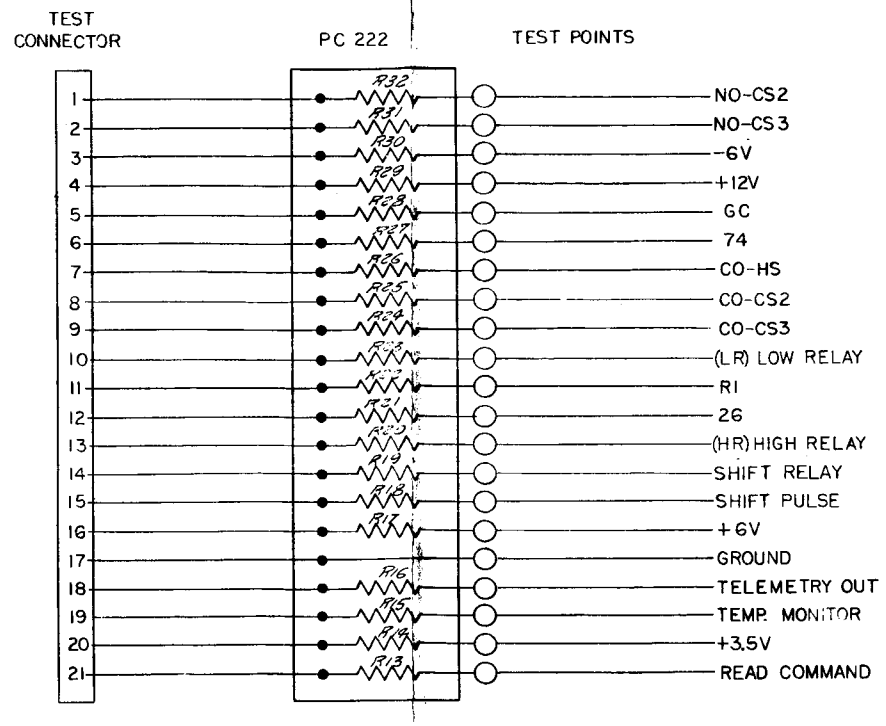
REV	DATE	BY	DESCRIPTION	APPVD





SECTION A-A





CIRCUIT COMPONENT LIST

FIND NO.	NO. REQD	DESCRIPTION	REMARKS
1	21	RESISTOR 4.3K 1/4W ±5%	WELWYN
2	1	CONNECTOR W/WIRES MDB1-21SH001	CANNON

NOTES:
1. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

WTA 2158-D-495

2158-B-501 NEXT ASSY.	USED ON APPLICATION	MATERIAL	NAME	INIT	DATE
		DO NOT SCALE THIS DRAWING	DESIGNER		
		REMOVE BURRS, BREAK SHARP EDGES	DRAWN WTA		
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED		
		TOLERANCE ON FRACTIONS ±	SCALE: 4:1	APPROVED	
		DECIMALS ±.005, ANGLES ±	FINISH:	APPROVED	
			CLIENT:		

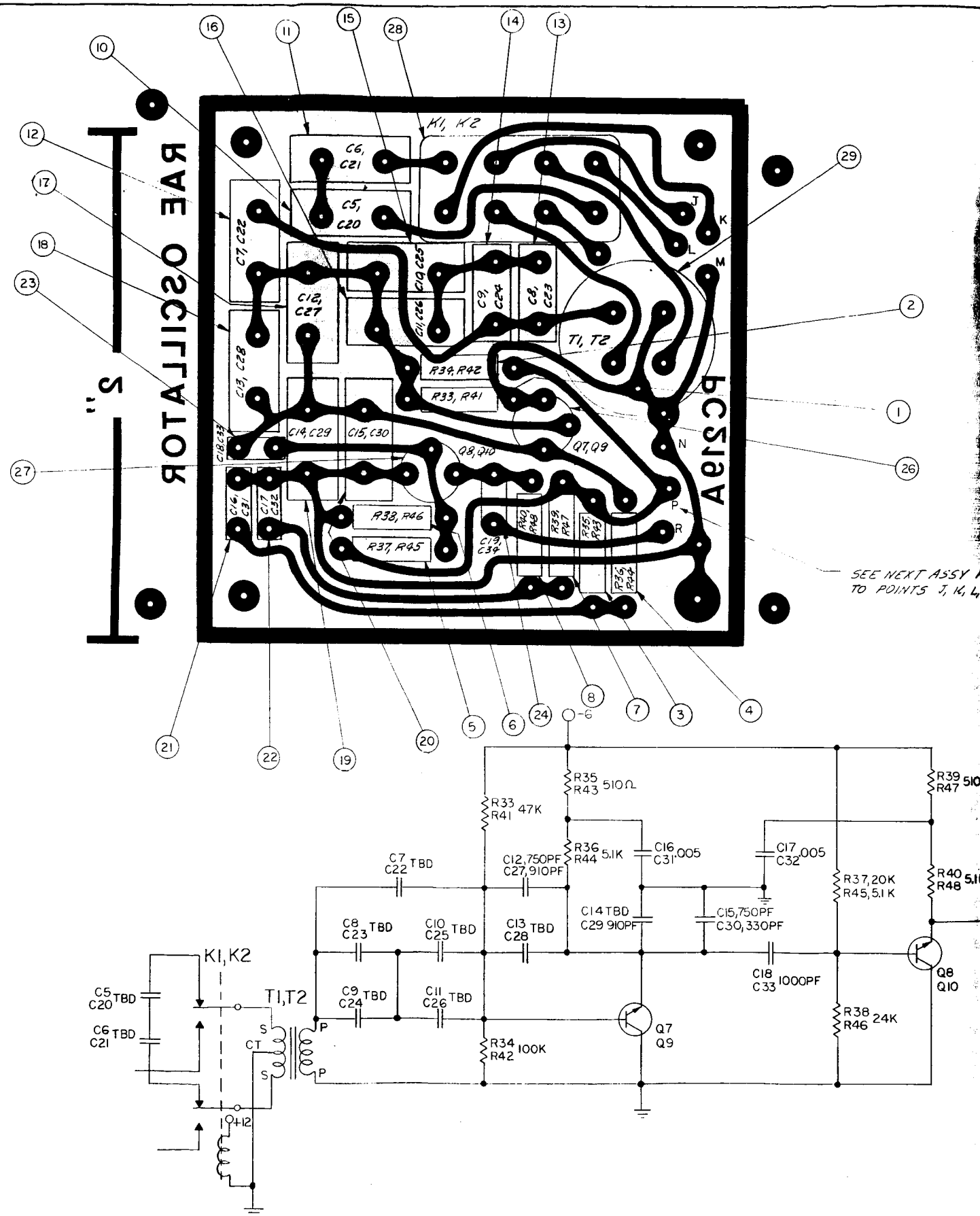
RAE
PRINTED WIRING ASSY.
TEST LIMITER

SCALE | UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-1155-204

CODE | SHEET 1 OF 1



REV	DATE	BY	DESCRIPTION	APPVD

NOTES:

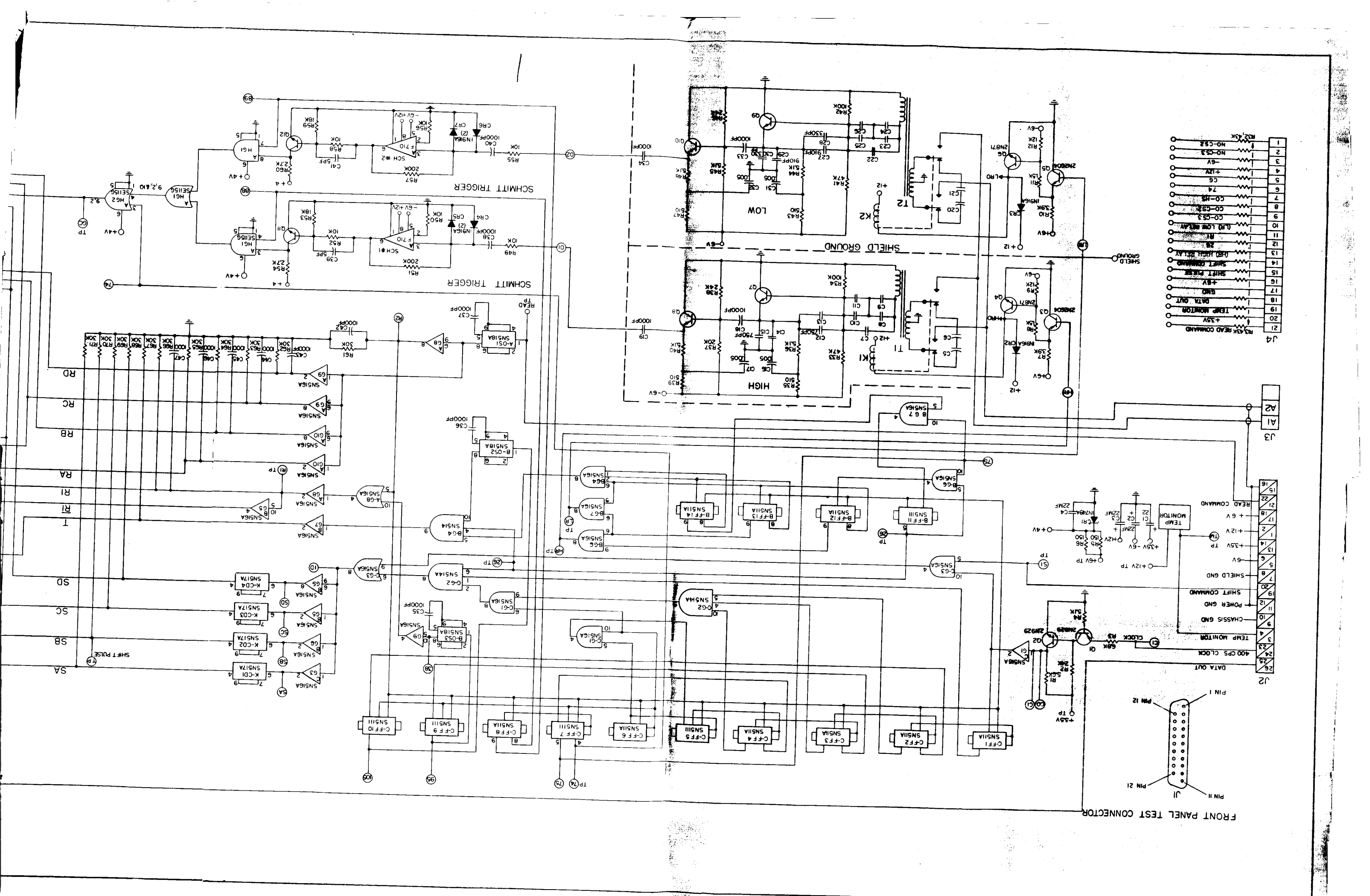
1. THIS DRAWING APPLIES FOR BOTH OSCILLATOR 1 & 2. CHECK LIST OF COMPONENTS FOR VALUE DIFFERENCES.
2. SEE NEXT ASSEMBLY FOR INTER-BOARD WIRING.
3. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4

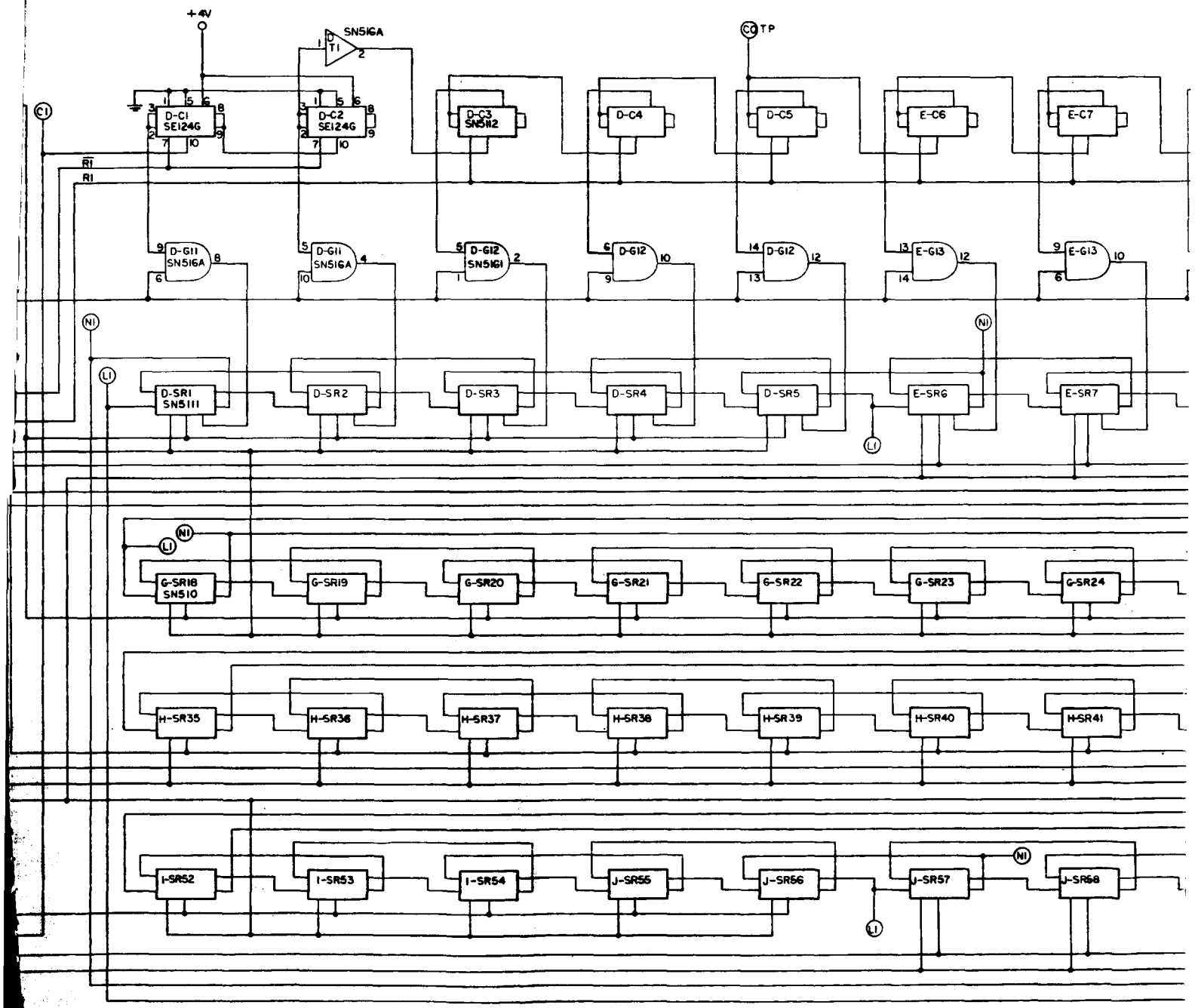
LIST OF COMPONENTS

FOR BOTH ITEM	FOR BOTH REQ'D	-I USED IN HIGH OSC.	-I DESCRIPTION	-II USED IN LOW OSC	-II DESCRIPTION	REMARKS FOR BOTH
1	1	R33	RESISTOR, 47K 1/4W ±5%	R41	RESISTOR, 47K 1/4W ±5%	WELWYN
2	1	R39	100K	R42	100K	
3	1	R35	510Ω	R43	510Ω	
4	1	R36	5.1K	R44	5.1K	
5	1	R37	20K	R45	5.1K	
6	1	R38	24K	R46	24K	
7	1	R39	510Ω	R47	510Ω	
8	1	R40	RESISTOR, 5.1K 1/4W ±5%	R48	RESISTOR, 5.1K 1/4W ±5%	WELWYN
9						
10	1	C5	CAPACITOR, TO BE DETERM.	C20	CAPACITOR, TO BE DETERM.	
11	1	C6		C21		
12	1	C7		C22		
13	1	C8		C23		
14	1	C9		C24		
15	1	C10		C25		
16	1	C11	TO BE DETERM.	C26	TO BE DETERM	
17	1	C12	750PF DN15	C27	330PF DN15	ELMENCO
18	1	C13	TBD	C28	TBD	
19	1	C14	TBD	C29	910PF DN15	ELMENCO
20	1	C15	750PF DN 15	C30	330PF	ELMENCO
21	1	C16	.005MFD	C31	.005MFD	CENTRALAB
22	1	C17	.005MFD	C32	.005MFD	CENTRALAB
23	1	C18	1000PF	C33	1000PF	VITRAMON
24	1	C19	CAPACITOR, 1000PF	C34	CAPACITOR, 1000PF	VITRAMON
25						
26	1	Q7	TRANSISTOR, 2N915	Q9	TRANSISTOR 2N915	MOT
27	1	Q8	TRANSISTOR 2N915	Q10	TRANSISTOR 2N915	MOT
28	1	K1	RELAY	K1	RELAY	
29	1	T1	TRANSFORMER (B-568) WTA	T2	TRANSFORMER (B-569)	WTA

WTA 2158-D-506

2158-R-501 NEXT ASSY.	USED ON APPLICATION	MATERIAL -	DO NOT SCALE THIS DRAWING REMOVE BURRS, BREAK SHARP EDGES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS ± DECIMALS ± . ANGLES ±	SCALE: 4:1 FINISH: CLIENT:	NAME / INIT / DATE DESIGNER DRAWN WTA CHECKED APPROVED APPROVED	RAE PRINTED WIRING ASS'Y RAE OSCILLATOR	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND GD-RAE-1155-205 SCALE / UNIT WT / CODE / SHEET 1 OF 1


SCHMITT TRIGGER
SCHMITT TRIGGER
SHIELD GROUND
LOW
HIGH
K2
K1
T2
T1
J4
J3
J2
J1
TEMP MONITOR
400 CPS CLOCK
CHASSIS GND
POWER GND
SHIFT COMMAND
SHIELD GND
+6V
+12V
+35V
READ COMMAND
DATA OUT
CLOCK
FRONT PANEL TEST CONNECTOR
PIN 1
PIN 11
PIN 21
PIN 12
SHIFT PULSE
SA
SB
SC
SD
RA
RB
RC
RD
T
RI


+4V
SN5IGA
CO TP
CI
D-CI SE124G
D-C2 SE124G
D-C3 SN5112
D-C4
D-C5
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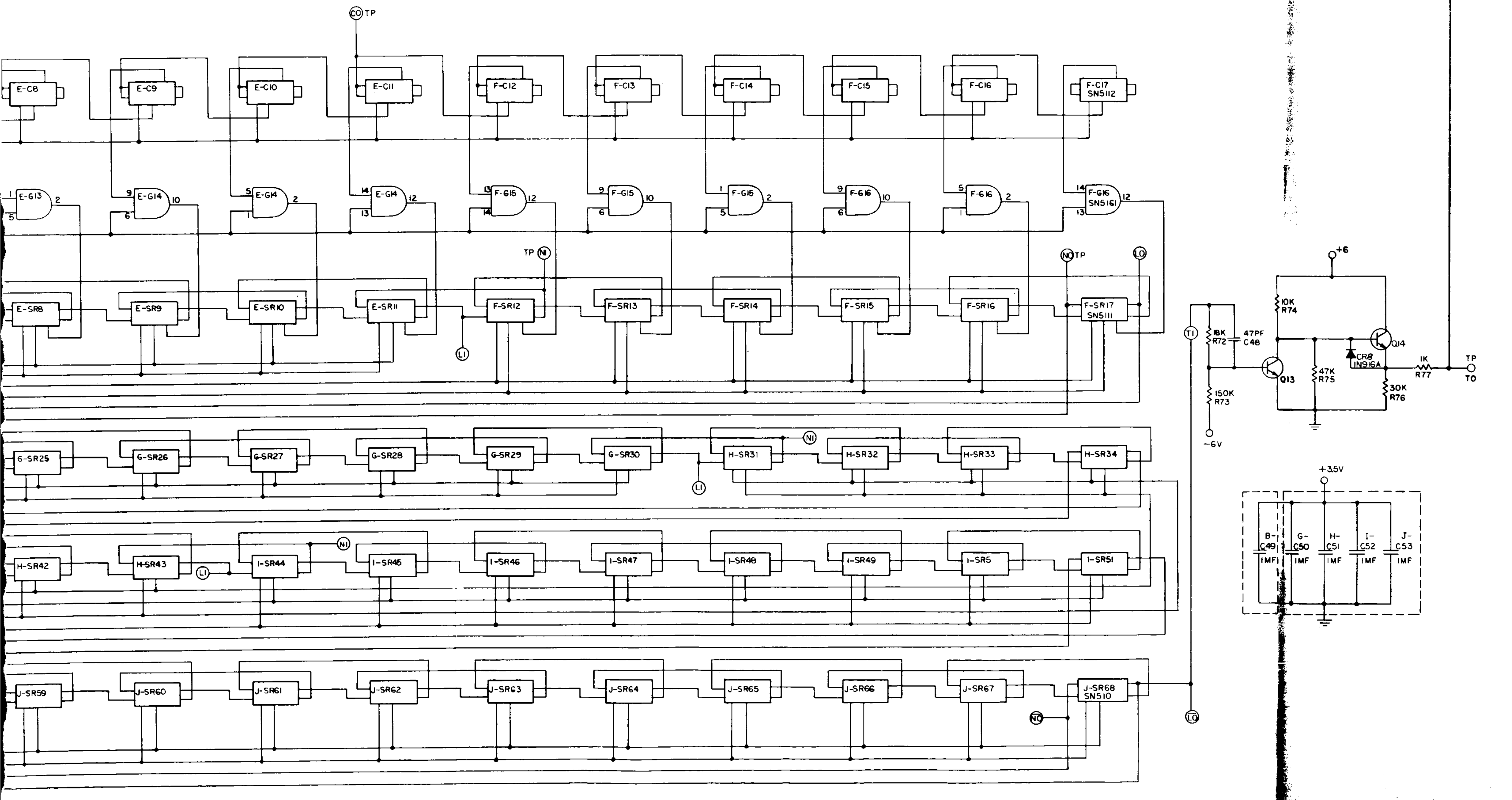
E-C7
RI
RI
D-GII SN5I6A
D-GII SN5I6A
D-GI2 SN5IGI
D-GI2
D-GI2
E-GI3
E-GI3
NI
LI
D-SRI SN5III
D-SR2
D-SR3
D-SR4
D-SR5
E-SR6
E-SR7
LI
NI
LI
G-SRI8 SN510
G-SRI9
G-SR20
G-SR2I
G-SR22
G-SR23
G-SR24
H-SR35
H-SR36
H-SR37
H-SR38
H-SR39
H-SR40
H-SR4I
I-SR52
I-SR53
I-SR54
J-SR55
J-SR56
J-SR57
J-SR58
NI
LI



3

NOTES:
1. ALL WELWYN RESISTORS ARE TYPE F25, LEADS GOLD PLATED DUMET .025 DIA
2. COMPONENTS LISTED FOR REFERENCE ONLY.

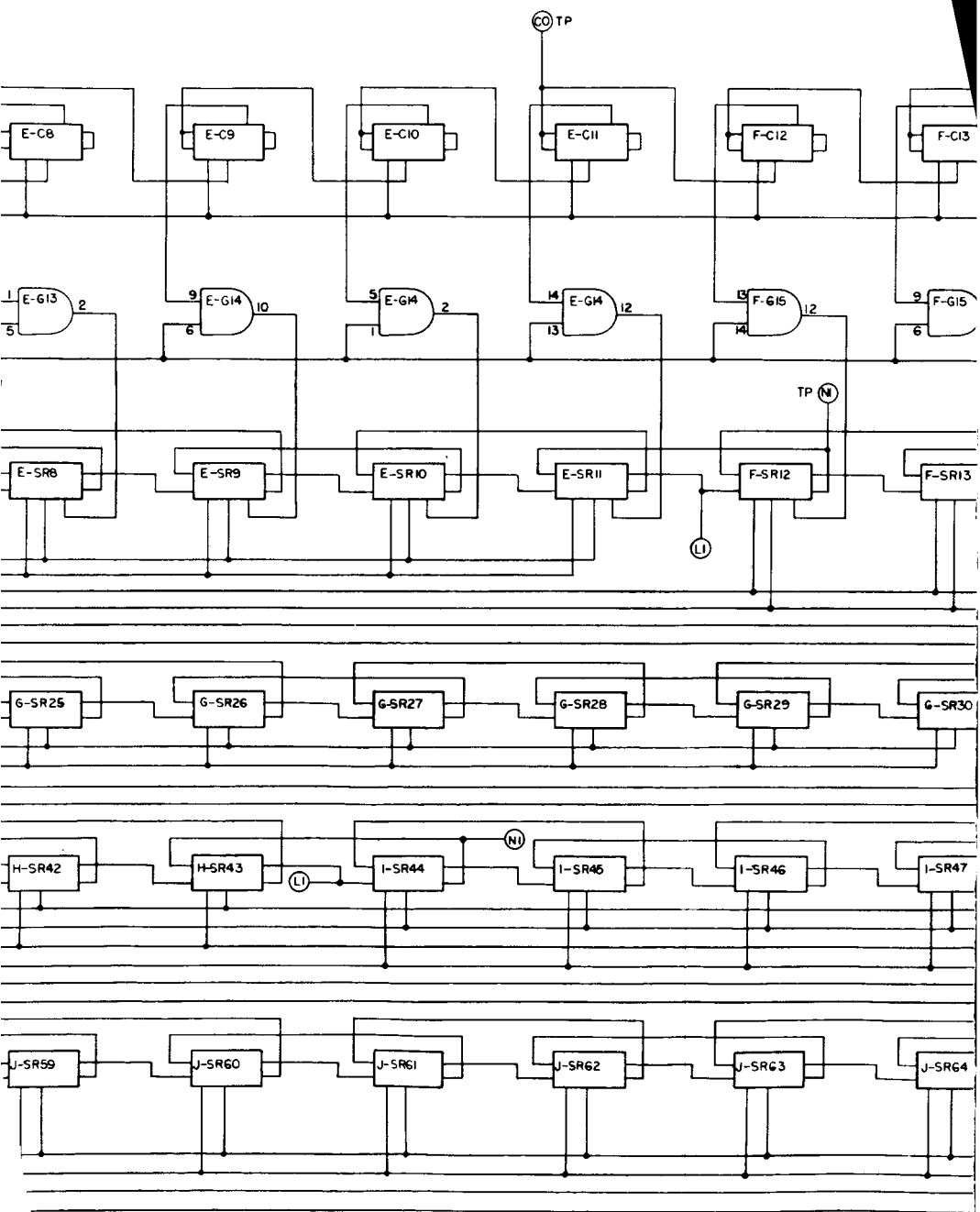
ITEM	REQD	DESIGNATOR	DESCRIPTION, PART NO.	MFR
70	2	T1, T2	TRANSFORMER 2158-C-531	WTA
69	2	K1, K2	RELAY, BBD7IZCIPCAS	FILTORS INC.
68	2	R51, R57	RESISTOR, 200K 1/8W ± 1% DM	IRC
67	1	R73	150K 1/8W ± 1% DM	IRC
66	2	R34, R42	100K 1/4W ± 5%	WELWYN
65	3	R33, R41, R75	47K	
64	20	R13 THRU R32	43K	
63	12	R61 THRU R71, R76	30K	
62	3	R2, R38, R46	24K	
61	2	R37, R45	20K	
60	3	R53, R59, R72	18K	
59	2	R9, R12	12K	
58	7	R48, R50, R52, R55, R56, R58, R74	10K	
57	1	R1	5.6K	
56	6	R3, R36, R40, R44, R48, R4	5.1K	
55	2	R7, R10	3.9K	
54	2	R54, R60	2.7K	
53	2	R8, R11	1.5K	
52	1	R77	1K	
51	4	R35, R39, R43, R47	510Ω	
50	2	R5, R6	RESISTOR 150Ω 1/4W ± 5%	WELWYN
49				
48				
47	1	C14	CAPACITOR, NOT USED	
46	1	C13	NOT USED	
45	1	C26	TBD	
44	1	C25		
43	1	C24		
42	1	C23		
41	1	C22		
40	1	C21		
39	1	C20		
38	1	C11		
37	1	C10		
36	1	C9		
35	1	C8		
34	1	C7		
33	1	C6		
32	1	C5	TBD	
31	1	C3	22 MFD 35 VDC 350D 20%	SPRAGUE
30	3	C1, C2, C4	22 MFD 15 VDC 350D 20%	SPRAGUE
29	5	C49 THRU C53	1 MFD 15 VDC 350D 20%	SPRAGUE
28	4	C16, C17, C31, C32	.005 MFD VK 30CW562K	VITRAMON
27	15	C35 THRU C38, C40, C42 THRU C47, C18, C19, C33, C34	1000 PF, VK 20CW102	VITRAMON
26	2	C27, C29	910 PF DM 15 SERIES	ELMENCO
25	2	C12, C15	750 PF DM 15	ELMENCO
24	2	C28, C30	330 PF DM 15	ELMENCO
23	1	C48	47 PF MC 80 SERIES	AEROVOX
22	2	C39, C41	CAPACITOR, 5 PF MC 80 SERIES	AEROVOX
21				
20	7	CR2 THRU CR8	DIODE IN916A	T.I.
19	1	CR1	DIODE IN749A	T.I.
18	1	Q11, Q12	TRANSISTOR 2N3052	T.I.
17	4	Q7 THRU Q10	2N915	MOTOROLA
16	2	Q4, Q6	2N871	FAIRCHILD
15	2	Q3, Q5	2N2604	T.I.
14	2	Q1, Q2	TRANSISTOR 2N929	T.I.
13	2	Q13, Q14	TRANSISTOR 2N930	T.I.
12	2	SCH1, SCH2	AMPLIFIER μA 710	FAIRCHILD
11	2	HC1, HC2	DTL DUAL NAND/NOR SE115G	SIGNETICS
10	2	C1, C2	BINARY ELEMENT SE124G	SIGNETICS
9	5	G11 THRU G15	NAND-NOR GATE SN5161	T.I.
8	3	OS1 THRU OS3	ONE SHOT SN518A	T.I.
7	4	CD1 THRU CD4	CLOCK DRIVER SN517A	T.I.
6	8	G1, G3, G5 THRU G10	DUAL 4 INPUT NAND-NOR G. SN516A	T.I.
5	2	G2, G4	DUAL 8 INPUT NAND-NOR G. SN514A	T.I.
4	15	C3 THRU C17	RIPPLE-COUNTER F-F SN5112	T.I.
3	9	FF1 THRU FF4, FF6, FF8, FF12 THRU FF14	R/S FLIP-FLOP COUNTER SN5114	T.I.
2	28	FF5, FF7, FF9 THRU FF11, SR1-SR17	R/S FLIP-FLOP SN5111	T.I.
1	51	SR18 THRU SR68	R/S FLIP-FLOP COUNTER SN5110	T.I.
ITEM	REQD	DESIGNATOR	DESCRIPTION, PART NO.	MFR

WTA 2158-R-529

RAE
SCHEMATIC DIAGRAM
RAE-CAPACITANCE
PROBE EXPERIMENT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GR-RAE-1155-206


CO TP
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E-C9
E-C10
E-C11
F-C12
F-C13
E-G13
E-G14
E-G14
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F-G15
F-G15
TP NI
E-SR8
E-SR9
E-SR10
E-SR11
F-SR12
F-SR13
LI
G-SR25
G-SR26
G-SR27
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LI
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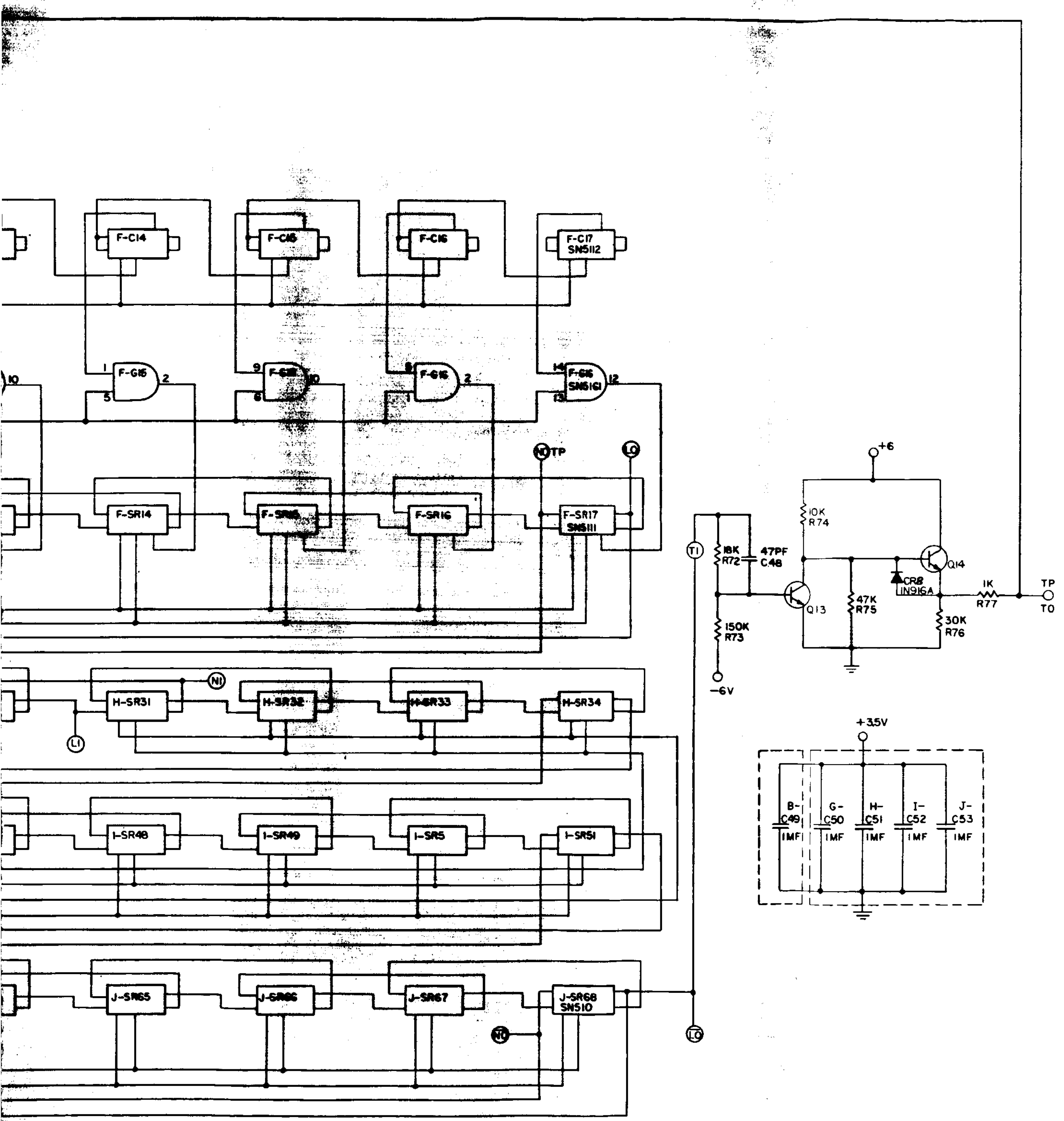
J-SR64



NOTES:
1. ALL WELWYN RESISTORS ARE TYPE F25, LEADS GOLD PLATED DUMET .025 DIA
2. COMPONENTS LISTED FOR REFERENCE ONLY.

ITEM	REQD	DESIGNATOR	DESCRIPTION, PART NO.	MFR
70	2	T1, T2	TRANSFORMER 2158-C-531	WTA
69	2	K, K2	RELAY, BRDTIZCIPCAS	FILTORS INC.
68	2	R51, R57	RESISTOR, 200K 1/8W ± 1% DM	IRC
67	1	R73	150K 1/8W ± 1% DM	IRC
66	2	R34, R42	100K 1/4W ± 5%	WELWYN
65	3	R33, R41, R75	47K	
64	20	R13 THRU R32	43K	
63	12	R61 THRU R71, R76	30K	
62	3	R2, R38, R46	24K	
61	2	R37, R45	20K	
60	3	R53, R59, R72	18K	
59	2	R9, R12	12K	
58	7	R49, R50, R52, R55, R56, R58, R74	10K	
57	1	R1	5.6K	
56	6	R3, R36, R40, R44, R48, R4	5.1K	
55	2	R7, R10	3.9K	
54	2	R54, R60	2.7K	
53	2	R8, R11	1.5K	
52	1	R77	1K	
51	4	R35, R39, R43, R47	510Ω	
50	2	R5, R6	RESISTOR 160Ω 1/4W ± 5%	WELWYN
49				
48				
47	1	C14	CAPACITOR, NOT USED	
46	1	C13	NOT USED	
45	1	C26	TBD	
44	1	C25		
43	1	C24		
42	1	C23		
41	1	C22		
40	1	C21		
39	1	C20		
38	1	C11		
37	1	C10		
36	1	C9		
35	1	C8		
34	1	C7		
33	1	C6		
32	1	C5	TBD	
31	1	C3	22 MFD 35 VDC 350D 20%	SPRAGUE
30	3	C1, C2, C4	22 MFD 15 VDC 350D 20%	SPRAGUE
29	5	C49 THRU C53	1 MFD 15 VDC 350D 20%	SPRAGUE
28	4	C16, C17, C31, C32	.005 MFD VK 30CW562K	VITRAMON
27	15	C35 THRU C38, C40, C42 THRU C47, C18, C19, C33, C34	1000 PF, VK 20CW102	VITRAMON
26	2	C27, C29	910 PF DM 15 SERIES	ELMENCO
25	2	C12, C15	750 PF DM 15	ELMENCO
24	2	C28, C30	330 PF DM 15	ELMENCO
23	1	C48	47 PF MC80 SERIES	AEROVOX
22	2	C39, C41	CAPACITOR, 5 PF MC 80 SERIES	AEROVOX
21				
20	7	CR2 THRU CR8	DIODE 1N916A	T.I.
19	1	CR1	DIODE 1N749A	T.I
18	1	Q11, Q12	TRANSISTOR 2N3052	T.I
17	4	Q7 THRU Q10	2N915	MOTOROLA
16	2	Q4, Q6	2N871	FAIRCHILD
15	2	Q3, Q5	2N2604	T.I
14	2	Q1, Q2	TRANSISTOR 2N929	T.I.
13	2	Q13, Q14	TRANSISTOR 2N930	T.I.
12	2	SCH1, SCH2	AMPLIFIER μA 710	FAIRCHILD
11	2	HC1, HC2	DTL DUAL NAND/NOR SE115G	SIGNETICS
10	2	C1, C2	BINARY ELEMENT SE124G	SIGNETICS
9	5	G11 THRU G15	NAND-NOR GATE SN5161	T.I.
8	3	OS1 THRU OS3	ONE SHOT SN518A	T.I.
7	4	CD1 THRU CD4	CLOCK DRIVER SN517A	T.I.
6	8	G1, G3, G5 THRU G10	DUAL 2 INPUT NAND-NOR G. SN516A	T.I.
5	2	G2, G4	DUAL 3 INPUT NAND-NOR G. SN5114A	T.I.
4	15	C3 THRU C17	RIPPLE-COUNTER F-F SN5112	T.I
3	9	FF1 THRU FF4, FF6, FF8, FF12 THRU FF14	R/S FLIP-FLOP COUNTER SN5114	T.I.
2	28	FF5, FF7, FF9 THRU FF11, SR1-SR17	R/S FLIP-FLOP SN5111	T.I.
1	51	SR18 THRU SR68	R/S FLIP-FLOP COUNTER SN5110	T.I.

WTA 2158-R-529

DO NOT SCALE THIS DRAWING
REMOVE BURRS, BREAK SHARP EDGES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS
DECIMALS ± ANGLES

APPLICATION: NEXT ASSY. / USED ON

DRAWN: WTA

RAE
SCHEMATIC DIAGRAM
RAE CAPACITANCE PROBE EXPERIMENT

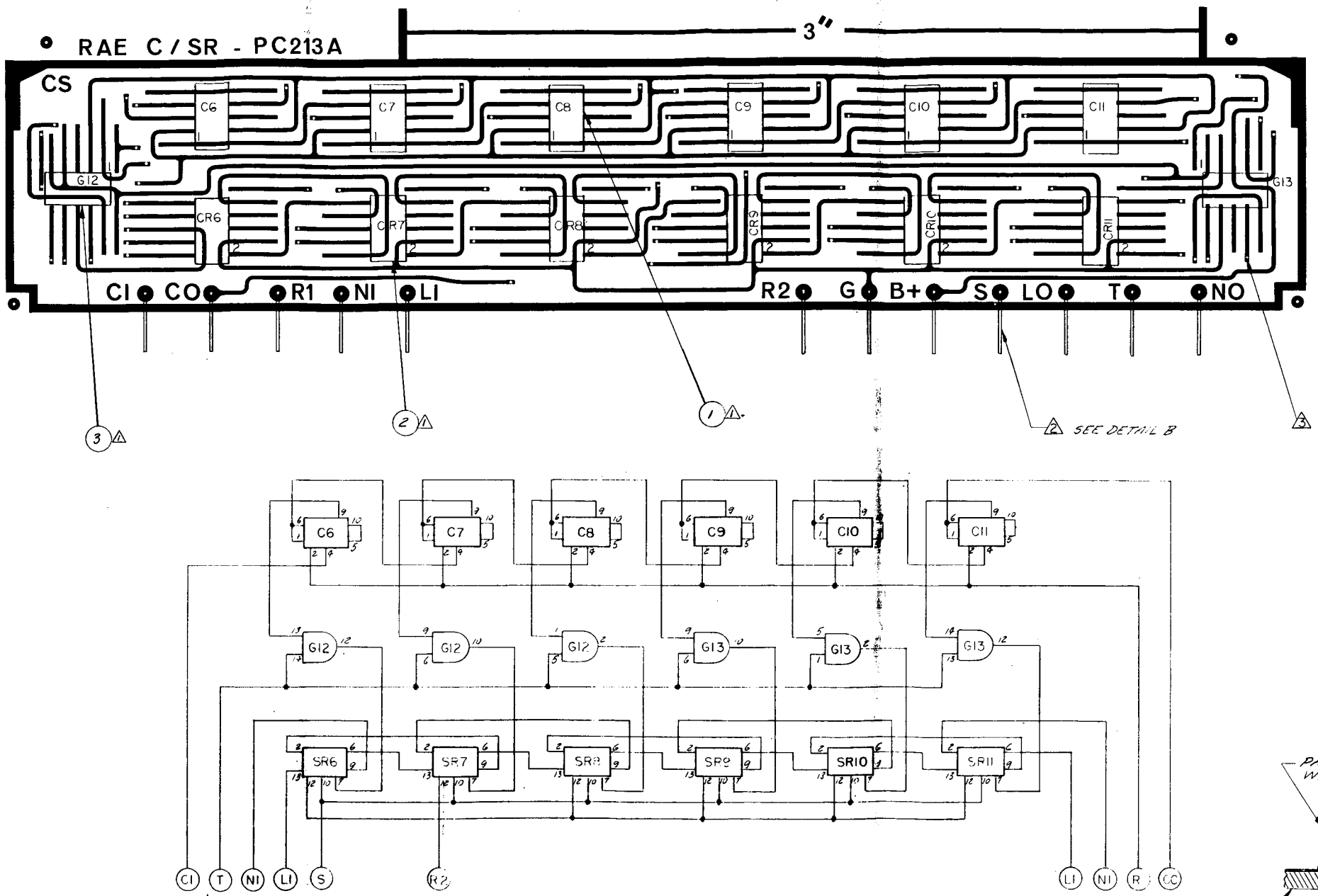
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GR-RAE-1155-206

SHEET 1 OF 1

3

REV	DATE	BY	DESCRIPTION	APPVD



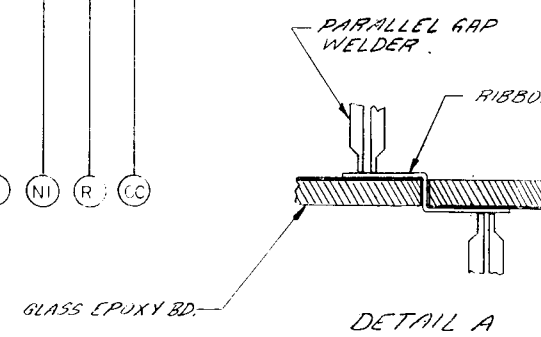
NOTE:
1. COMPONENT WIRING SHOWN FOR ASSY 1 ONLY FOR ASSY 2, REVERSE PINS 1 & 14.
2. STEP 1. INSTALL OUTPUT LEADS 0.020 GOLD DUMET
3. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS 62 PLACES. FEEDTHRU MATERIAL 0.01 X 0.004 KOVAR RIBBON
4. IN GATES (G) CUT-OFF PINS 7 AND 8. IN SHIFT REGISTERS (SR) CUT OFF PINS 1, 8, AND 14.
5. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

CIRCUIT COMPONENT LIST

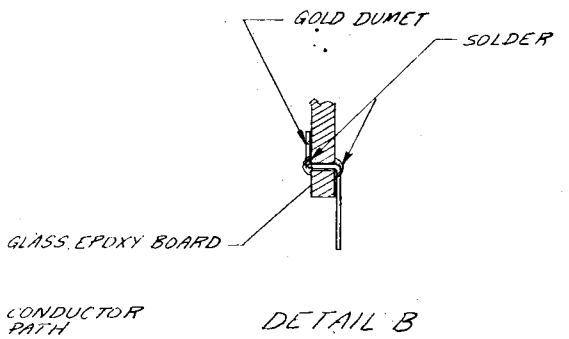
FIND NO	NO. REQD	DESCRIPTION	REMARKS
1	6	SN5112 RIPPLE-COUNTER F.F.	T.I.
2	6	SN111 R-S FLIP-FLOP	T.I.
3	2	SN5161 NAND/NOR GATE	T.I.

TABLE OF ASSEMBLIES

FIND NO	REF. DESIGNATIONS -1	-2
1	C6 THRU C11	C12 THRU C17
2	CR6 THRU CR11	CR12 THRU CR17
3	G12 & G13	G14 & G15



DETAIL A

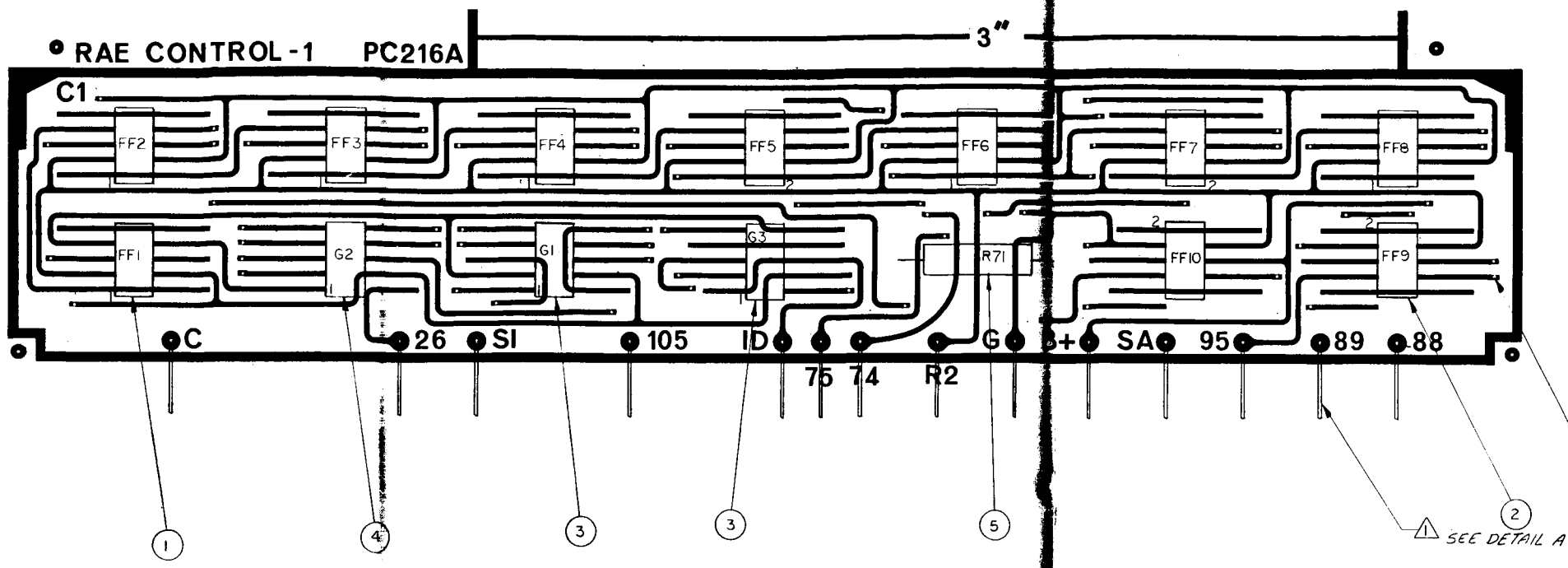


DETAIL B

WTA 2156 D 187

2158-59-501 NEXT ASSY. USED ON APPLICATION	MATERIAL	NAME	INIT	DATE	RAE PRINTED WIRING ASSY COUNTER SHIFT REGISTER	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		DESIGNER				
	DO NOT SCALE THIS DRAWING	DRAWN WTA				
	REMOVE BURRS, BREAK SHARP EDGES	CHECKED				
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS ± DECIMALS ± . ANGLES ±	SCALE: 4:1 APPROVED				GD-RAE-1155-102
		FINISH: APPROVED			SCALE	CODE
		CLIENT:			UNIT WT	SHEET 1 OF 1

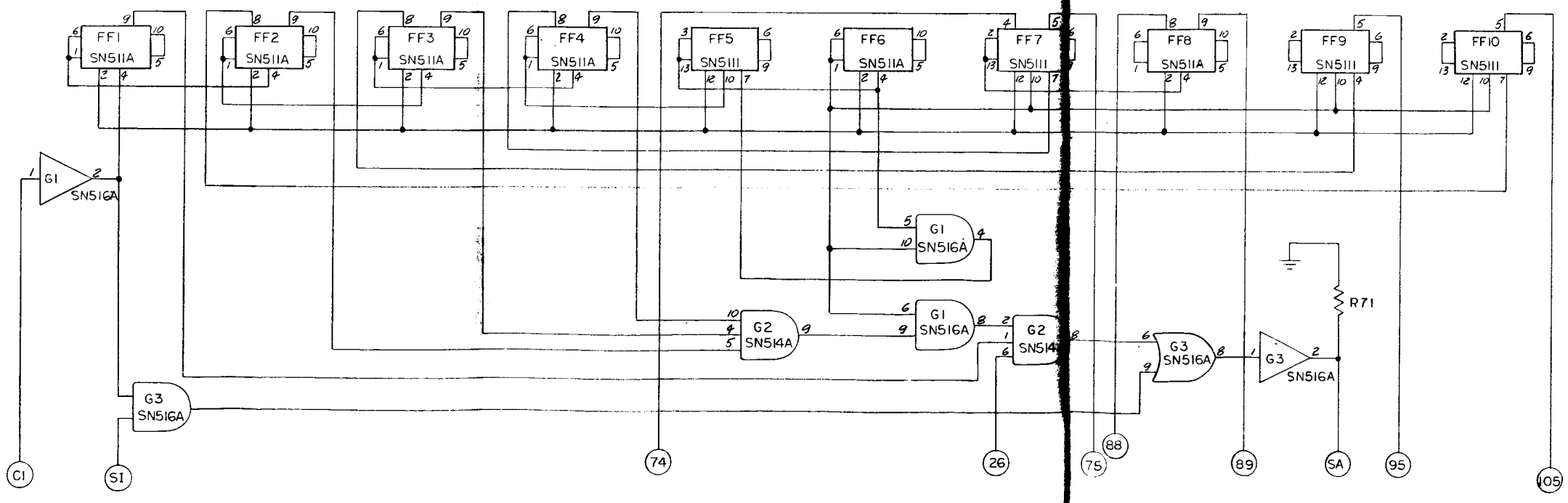
REV	DATE	BY	DESCRIPTION	APPVD

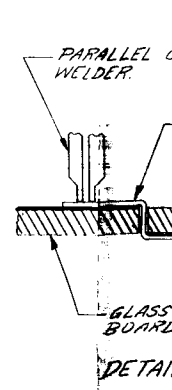


NOTES:
1. STEP 1. INSTALL OUTPUT LEADS: 0.020 GOLD DUMET
2. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS, 62 PLACES. FEEDTHRU MATERIAL 0.01 x 0.004 RODAR RIBBON.
3. IN FLIP-FLOPS (FF) 5, 7, 9, AND 10 CUTOFF 1, 8, AND 14 LEADS.
4. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

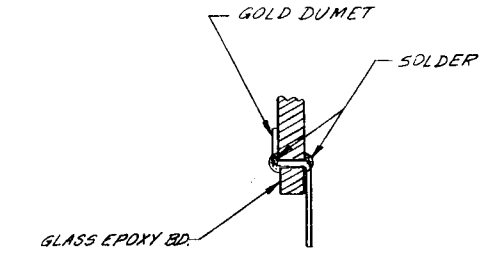
CIRCUIT COMPONENT LIST

FIND NO.	NO. REQD	DESCRIPTION	REMARKS
1	6	SN511A R-S FLIP-FLOP COUNTER	T.I.
2	4	SN5111 R-S FLIP-FLOP	T.I.
3	2	SN516A DUAL 2 INPUT NAND/NOR GATE	T.I.
4	1	SN514A DUAL 3 INPUT NAND/NOR GATE	T.I.
5	1	R71 RESISTOR,	A-B





DETAIL B



DETAIL A

WTA 2158 D-495

		MATERIAL	NAME	INIT	DATE
			DESIGNER		
		DO NOT SCALE THIS DRAWING	DRAWN WTA		
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED		
2158-F-501		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	APPROVED		
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± SCALE: 4:1	APPROVED		
APPLICATION		DECIMALS ± , ANGLES ± FINISH:			
		CLIENT:			

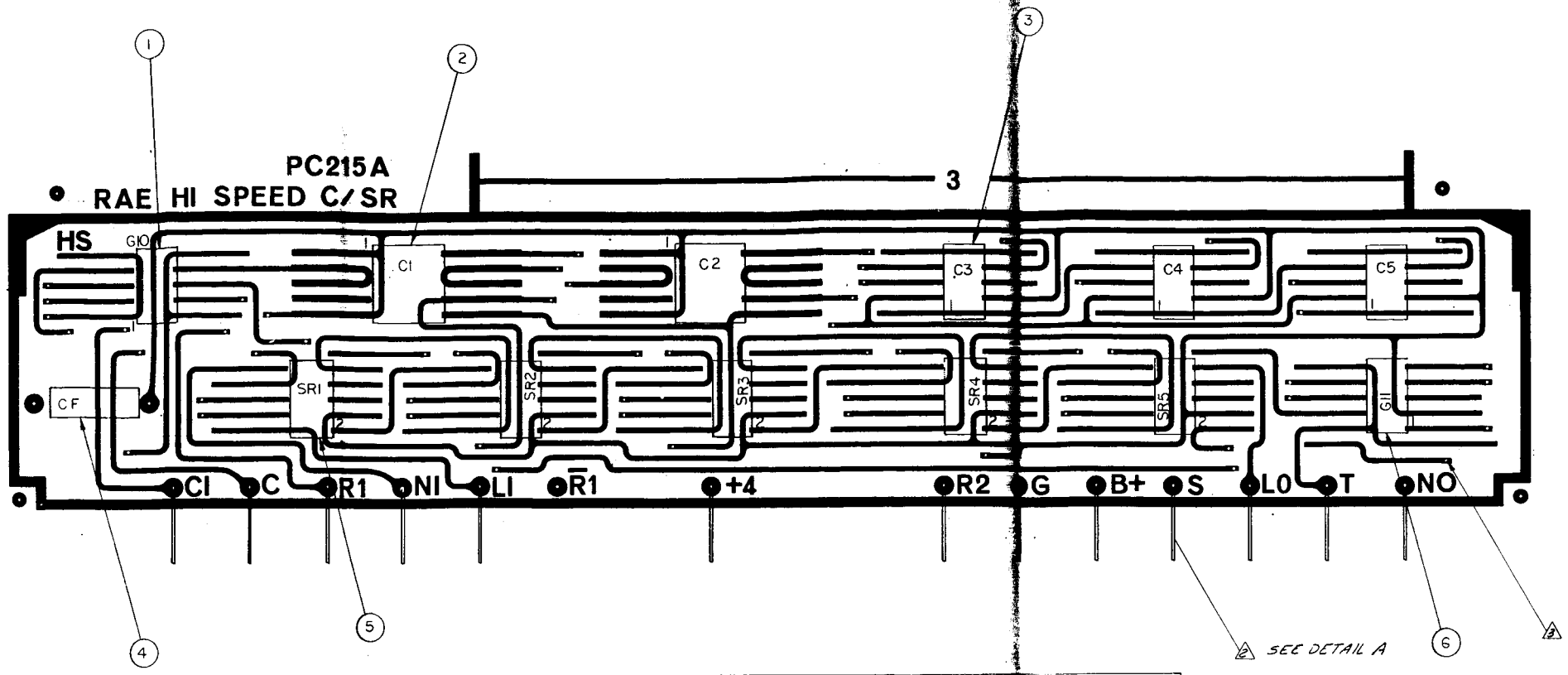
RAE
PRINTED WIRING ASSY
CONTROL CIRCUIT #1

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

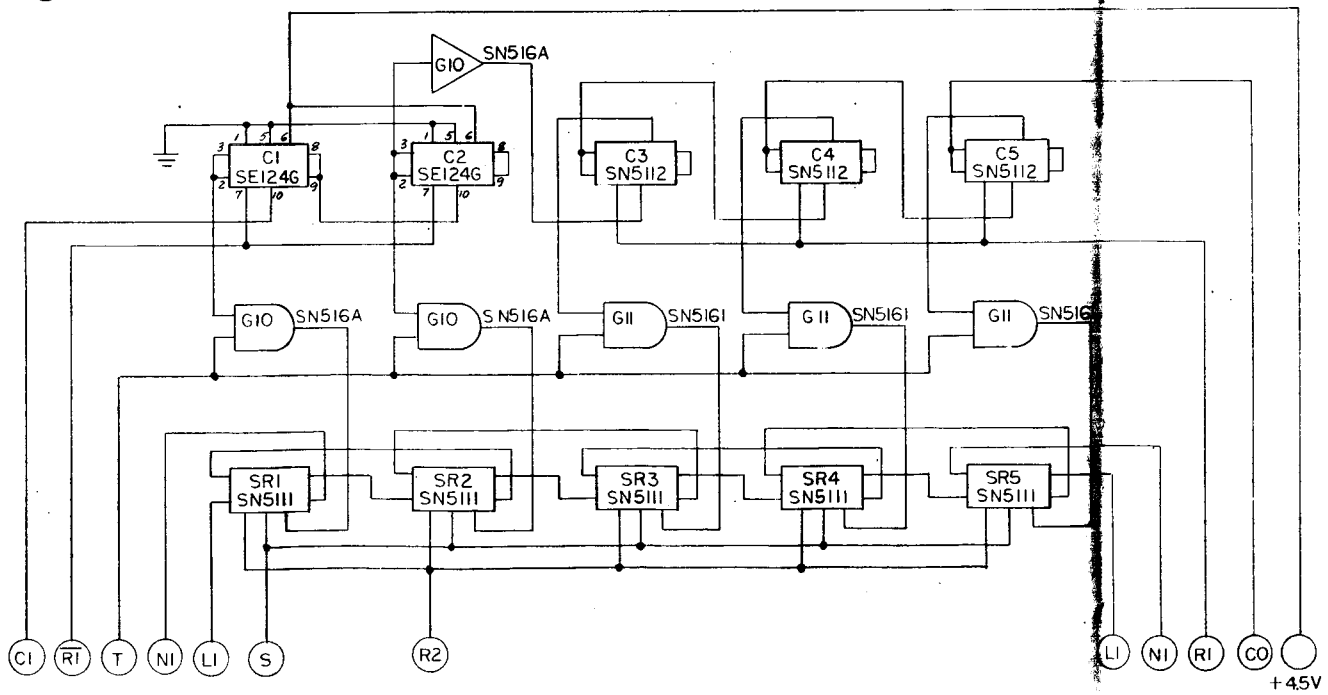
GD-RAE-1155-403

SCALE | UNIT WT | CODE | SHEET 1 OF 1

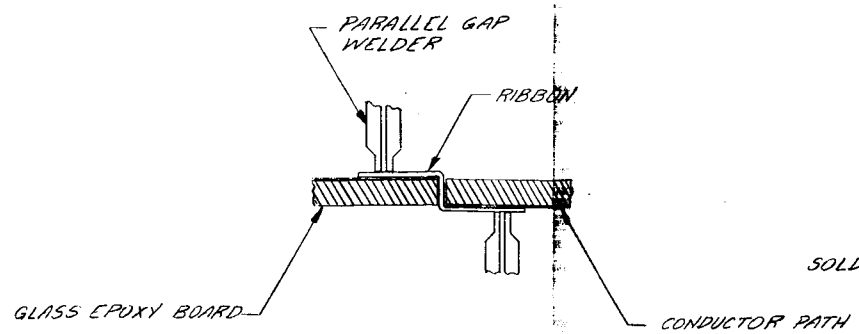
REV	DATE	BY	DESCRIPTION	APPVD



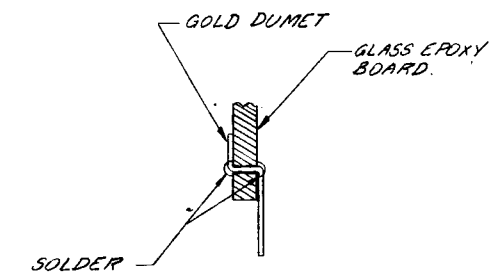
NOTES:
1. IN GATE 11 (G 11) CUT-OFF LEADS 7 & 8.
   IN ALL SHIFT REGISTERS (SR) CUT-OFF LEADS 1, 8, & 14.
2. STEP 1. INSTALL OUTPUT LEADS 0.020 GOLD DUMET.
3. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS. 58 PLACES. FEETHRU MATERIAL 0.01 x 0.004 RODAR RIBBON.
4. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.



CIRCUIT COMPONENT LIST			
FIND NO.	NO. REQ'D	DESCRIPTION	REMARKS
1	1	SN516A NAND/NOR GATE	T.I.
2	2	SE124G BINARY ELEMENT	SIGNETICS CORP.
3	3	SN5112 RIPPLE-COUNTER F-F	T.I.
4	1	CAPACITOR 150D 1 MFD 15VDC	SPRAGUE
5	5	SN5111 R-S FLIP-FLOP	T.I.
6	6	SN5161 NAND/NOR GATE	T.I.



DETAIL B



DETAIL A

WTA 2158-D-489

		MATERIAL		NAME	INIT	DATE
				DESIGNER		
		DO NOT SCALE THIS DRAWING		DRAWN WTA		
		REMOVE BURRS, BREAK SHARP EDGES		CHECKED		
2158-D-501		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1	APPROVED		
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± DECIMALS ± . ANGLES ±	FINISH:	APPROVED		
APPLICATION			CLIENT:			

RAE
PRINTED WIRING ASSY.
HS COUNTER
SHIFT REGISTER

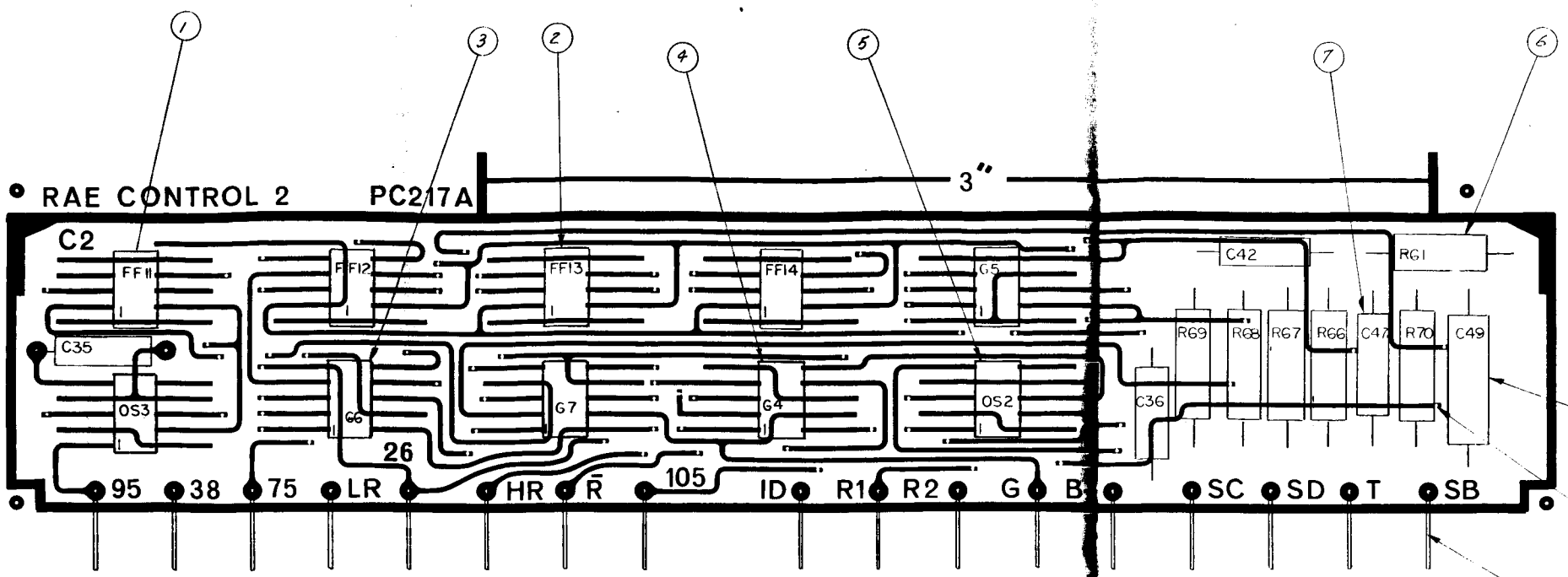
SCALE | UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-HS-404

CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD

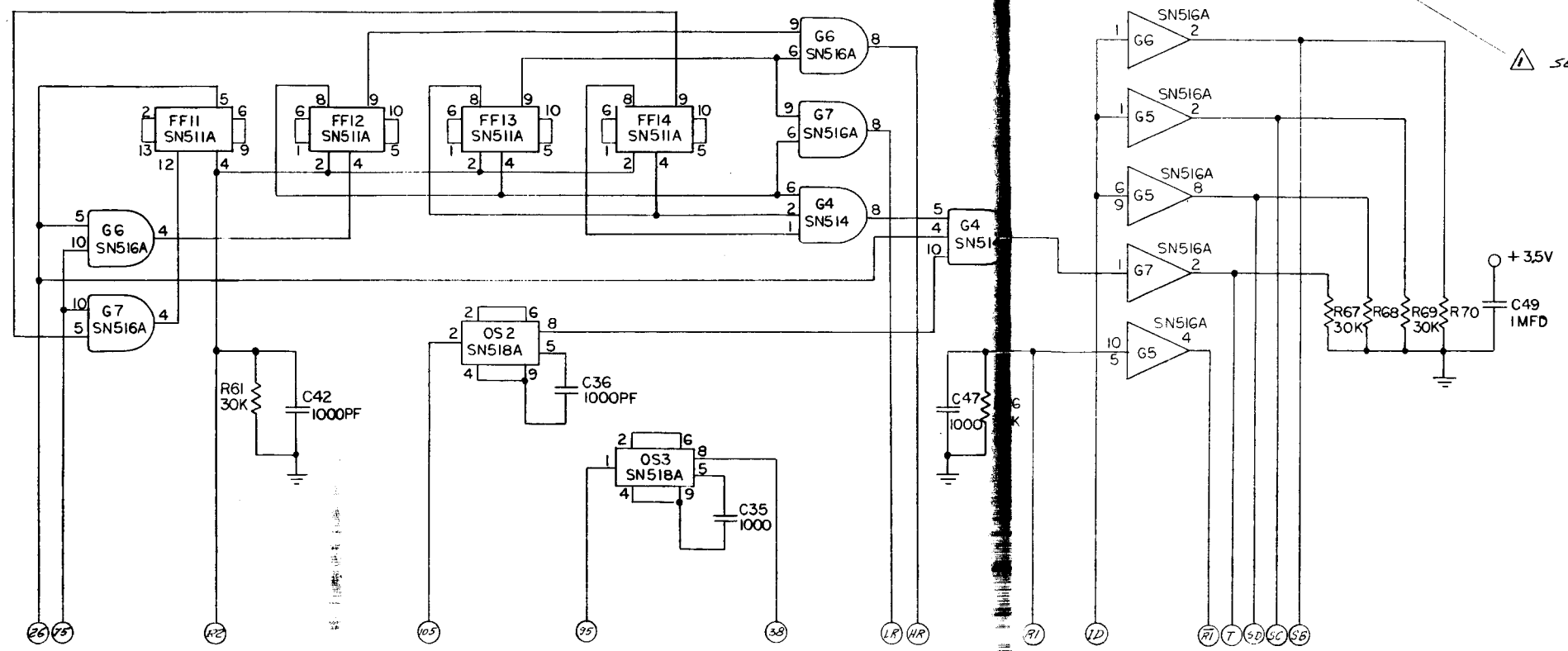


NOTES:
1. STEP 1. INSTALL OUTPUT LEADS 0.020 GOLD DUMET
2. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS, 76 PLACES. FEED THRU MATERIAL 0.04 x 0.004 RODAR RIBBON.
3. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.

⑧

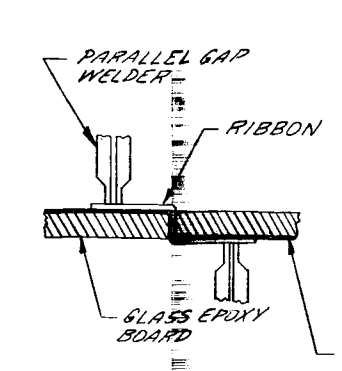
⑫ SEE DETAIL B

① SEE DETAIL A

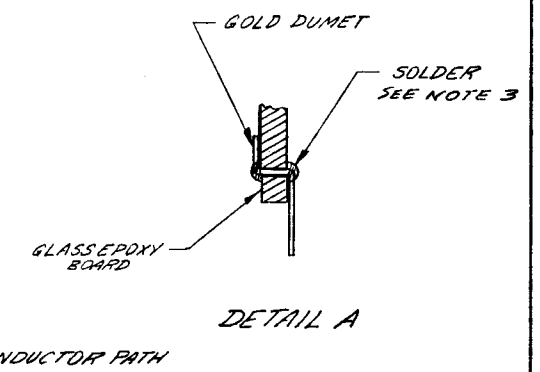


CIRCUIT COMPONENT LIST

FIND NO.	NO. REQD	DESCRIPTION	REMARKS
1	1	SN5111 R/S FLIP-FLOP	T.I.
2	3	SN511A R/S FLIP-FLOP COUNT.	T.I.
3	3	SN516A DUAL 2 INPUT NAND-NOR	T.I.
4	1	SN5114A DUAL 3 INPUT -"-	T.I.
5	2	SN518A ONE SHOT	T.I.
6	5	RESISTOR 30K, 1/4W ±5%	WELWYN
7	4	CAPACITOR, 1000 PF	VITRAMON
8	1	CAPACTOR, 1MFD 15V 150 D	SPRAGUE



DETAIL B

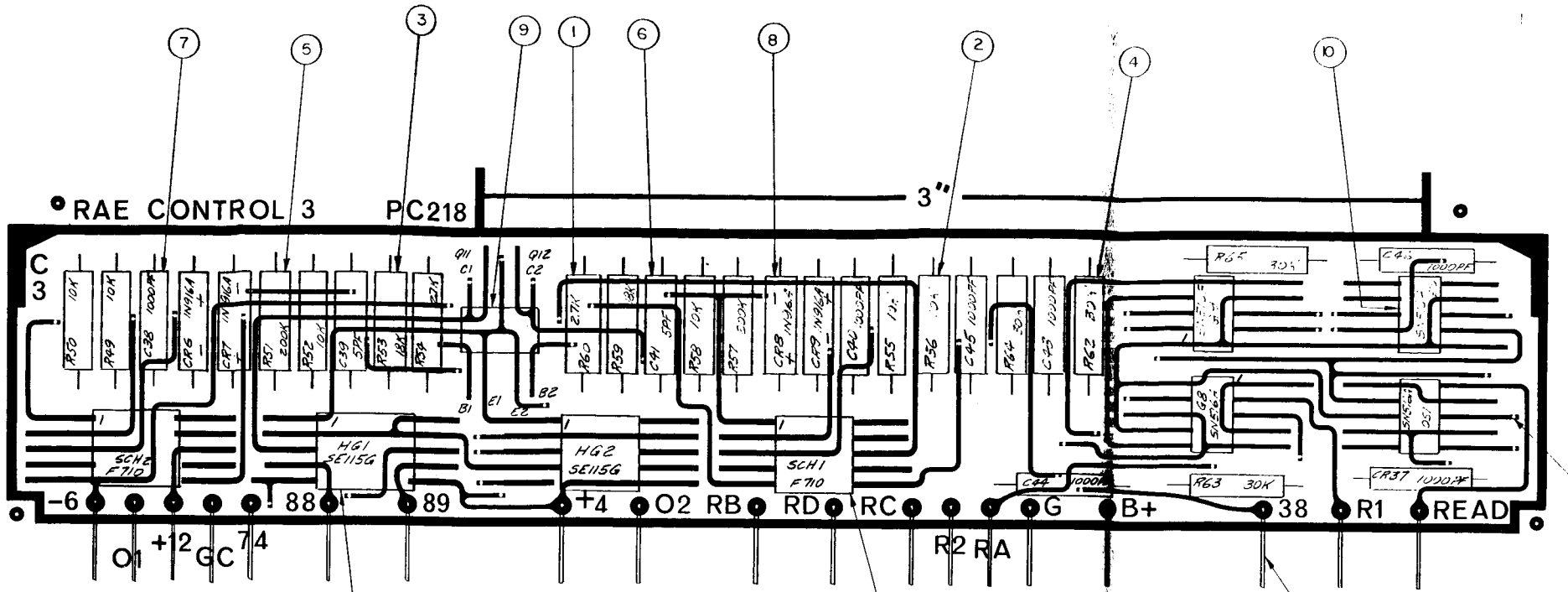


DETAIL A

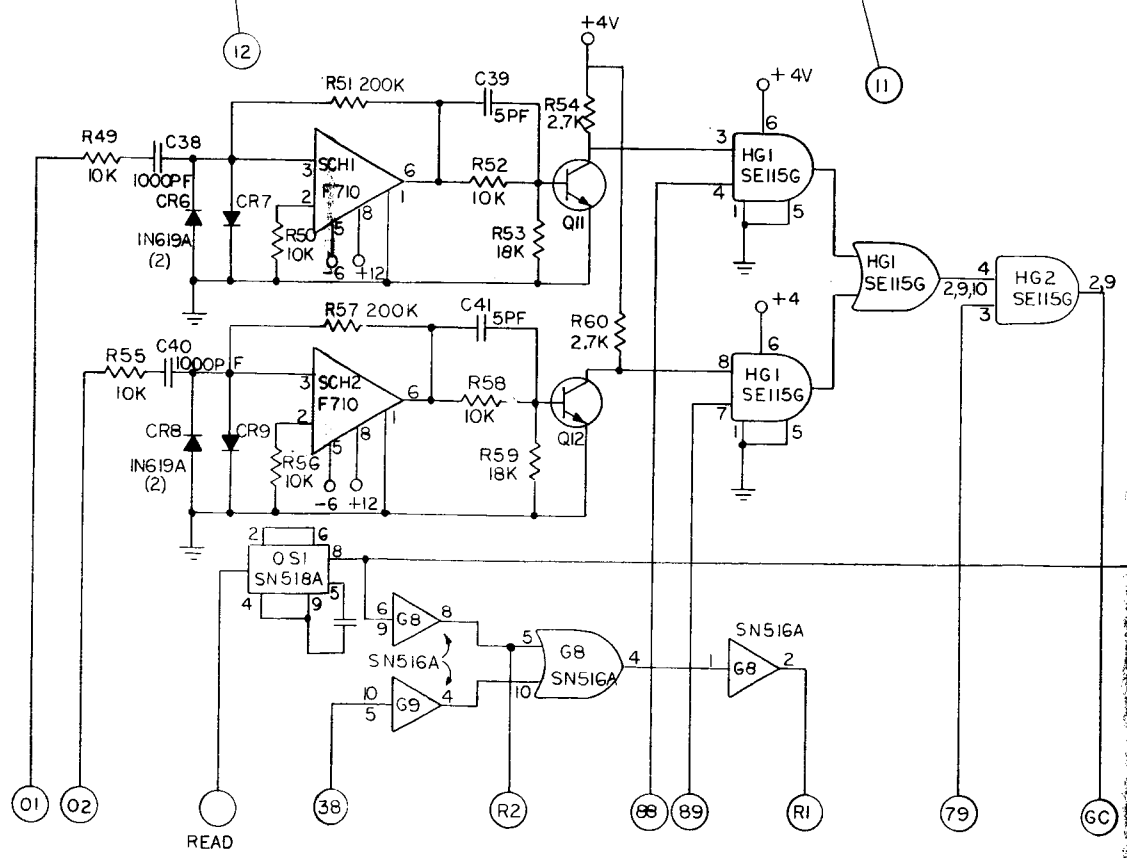
WTA 2158-D-499

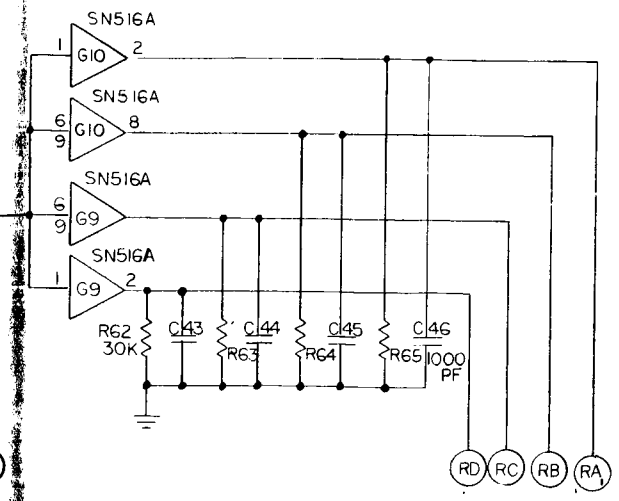
		MATERIAL	NAME	INIT	DATE		
			DESIGNER			RAE PRINTED WIRING ASSY CONTROL # 2	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		DO NOT SCALE THIS DRAWING	DRAWN WTA				
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED				
2158-R-501		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES SCALE: 4:1	APPROVED				GD-RAE-1155-405
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± DECIMALS .ANGLES ± FINISH:	APPROVED			SCALE	UNIT WT CODE SHEET 1 OF 1
APPLICATION		CLIENT:					

REV	DATE	BY	DESCRIPTION	APPVD



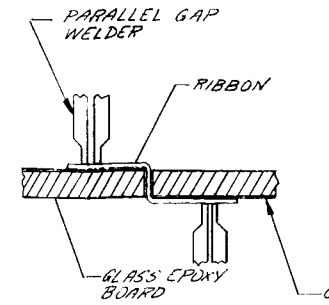
NOTES:
1. STEP 1. INSTALL OUTPUT LEADS 0.020 GOLD DUMET
2. STEP 2. WELDED FEEDTHRU TO BE INSTALLED PRIOR TO COMPONENTS, 50 PLACES. FEEDTHRU MATERIAL 0.001X0.004 RODAR RIBBON.
3. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4.



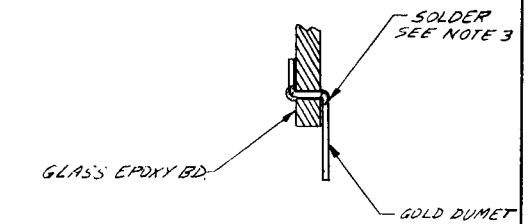


CIRCUIT COMPONENT LIST

FIND NO	NO. REQD	DESCRIPTION	REMARKS
1	2	RESISTOR 2.7K 1/4W ± 5%	WELWYN
2	6	10K	WELWYN
3	2	18K	WELWYN
4	4	30K	WELWYN
5	2	RESISTOR, 200K 1/4W ± 5%	IRC
6	2	CAPACITOR 5PF	AEROVOX
7	7	CAPACITOR 1000PF	VITRAMON
8	4	DIODE IN916A	
9	1	TRANSISTOR 2N3052	T.I
10	4	SN516A DUAL 2INPUT NAND-NOR G	T.I.
11	2	MA710 AMPLIFIER SCH 1, 2	FAIRCHILD
12	2	SE115G DTL DUAL NAND-NOR G	SIGNETICS



DETAIL B

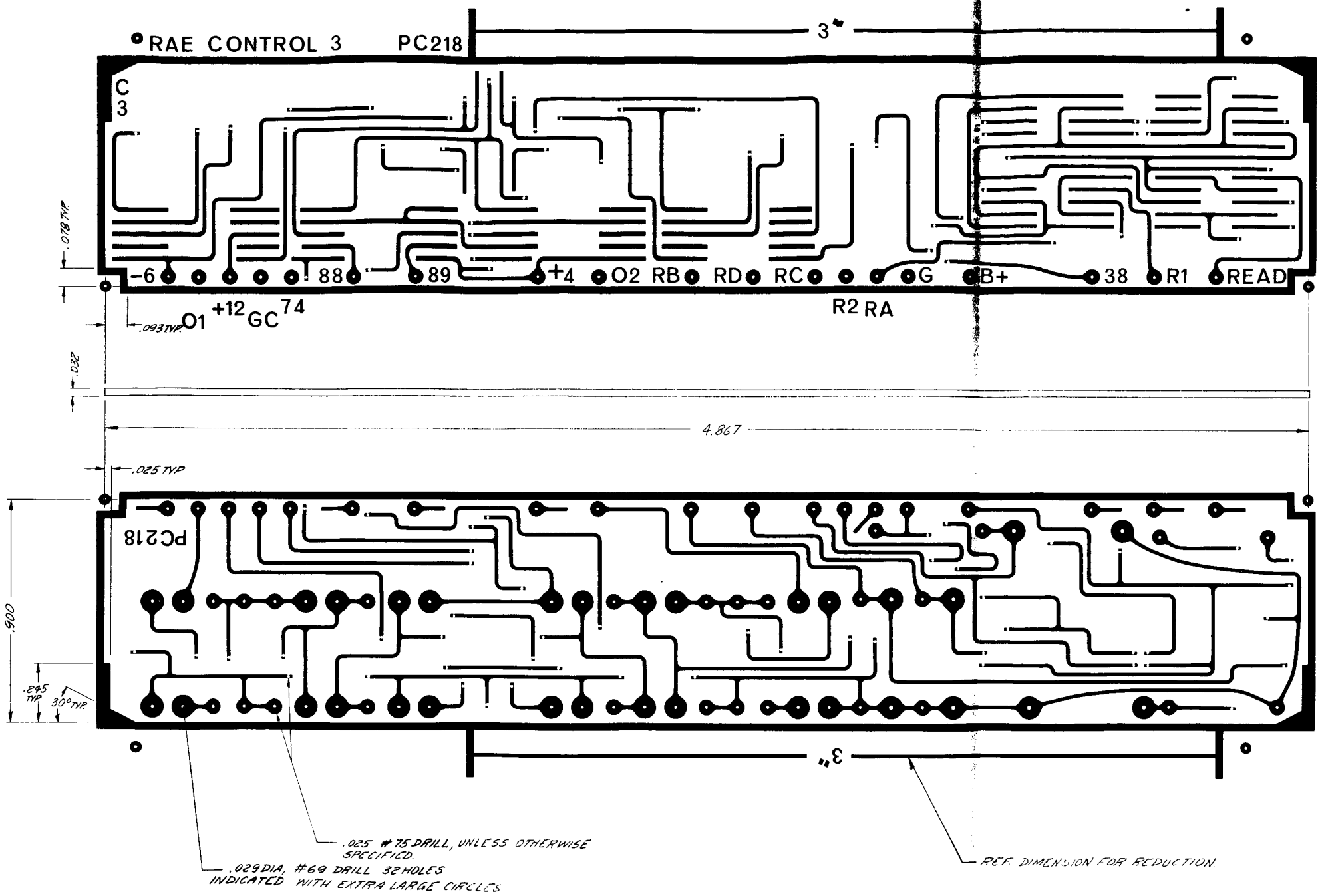


DETAIL A

WTA 2158-D 501

2158-E-501 NEXT ASSY.	USED ON APPLICATION	MATERIAL	NAME	INIT	DATE	RAE PRINTED WIRING ASSY. CONTROL #3
		DO NOT SCALE THIS DRAWING	DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		REMOVE BURRS, BREAK SHARP EDGES	DRAWN WTA			GD-RAE-1155-406
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED			
		TOLERANCE ON FRACTIONS · DECIMALS · ANGLES ·	APPROVED			
		SCALE: 4:1 FINISH: CLIENT:	APPROVED			SCALE · UNIT WT · CODE · SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD



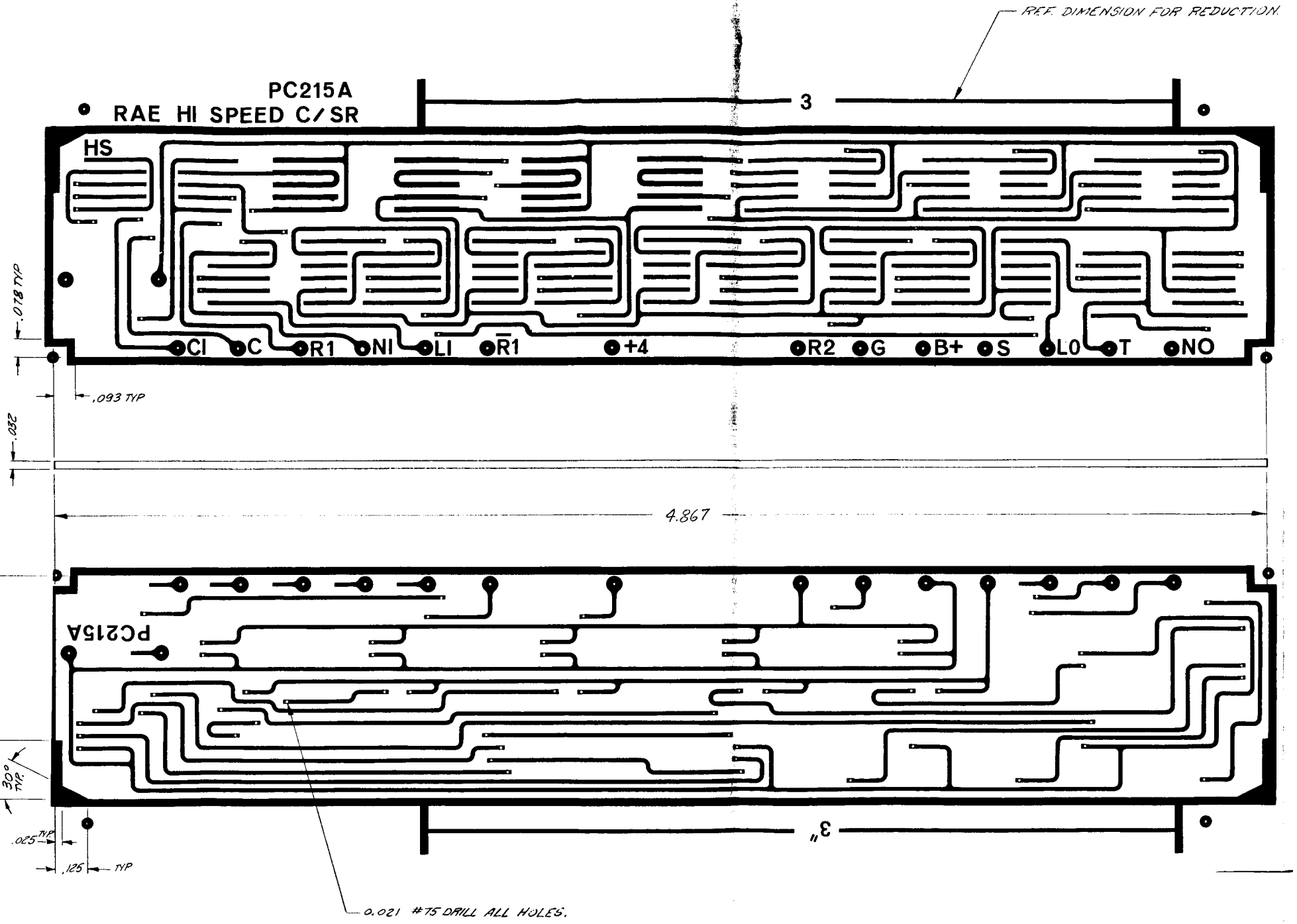
NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE.032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.

WTA 2158-D505

		MATERIAL SEE NOTE 1.	NAME	INIT	DATE	RAE PRINTED WIRING BOARD CONTROL #3
			DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
			DRAWN WTA			
		DO NOT SCALE THIS DRAWING	CHECKED			
		REMOVE BURRS, BREAK SHARP EDGES				
2158-D-502 NEXT ASSY.	USED ON APPLICATION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1			GD-RAE-1155-501
		TOLERANCE ON FRACTIONS ± DECIMALS ± .005, ANGLES ± 1°	FINISH:			
			CLIENT:			SCALE / UNIT WT / CODE / SHEET 1 OF 1
			APPROVED			
			APPROVED			

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FLGE.032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.

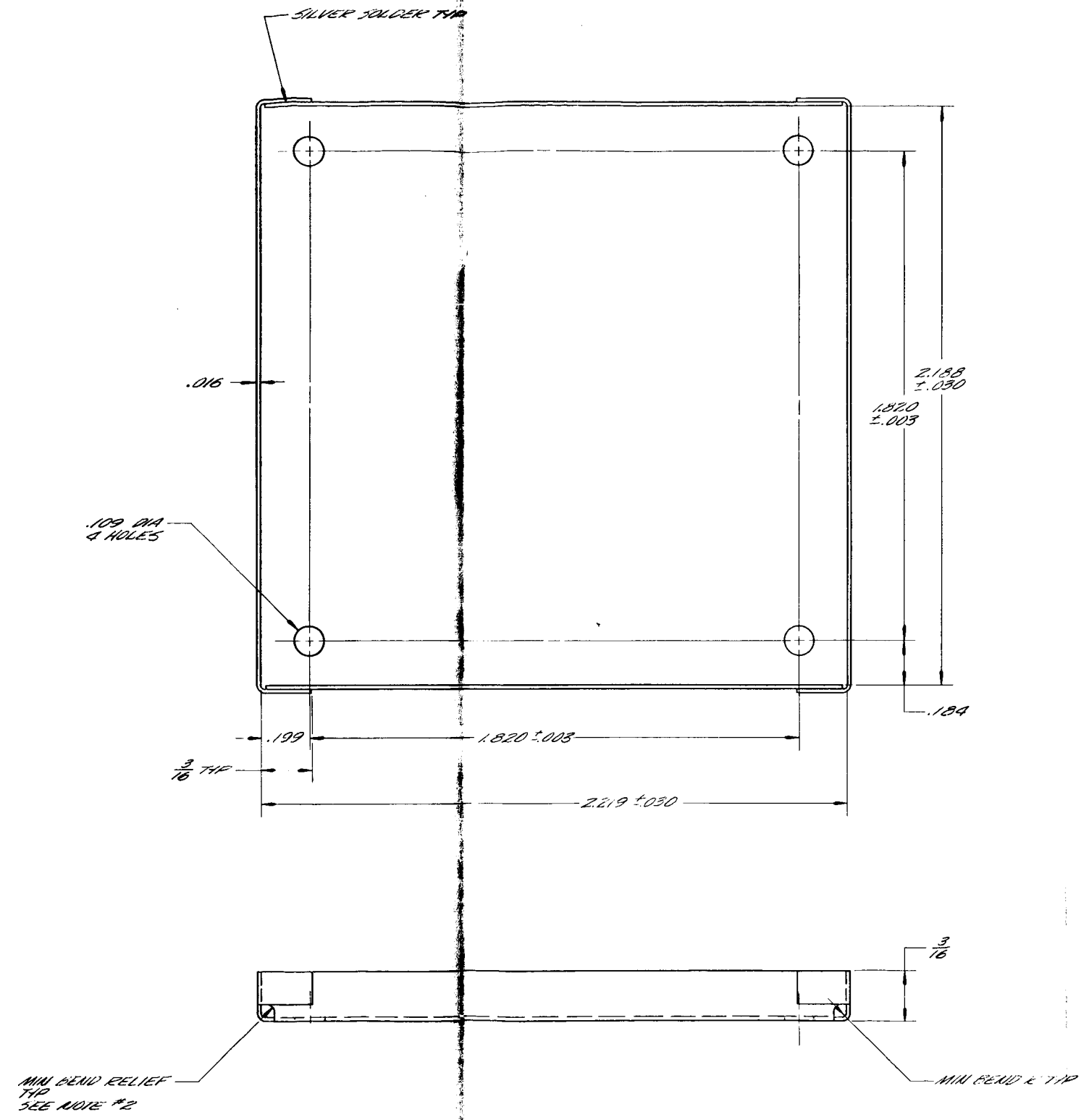
WTA 2158-D-490

		MATERIAL SEE NOTE 1.		NAME	INIT	DATE	RAE PRINTED WIRING BOARD H.S. COUNTER SHIFT REGISTER
		DO NOT SCALE THIS DRAWING		DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		REMOVE BURRS, BREAK SHARP EDGES		DRAWN WTA			
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4/1	CHECKED			
2158-D-489		TOLERANCE ON FRACTIONS ±	FINISH:	APPROVED			GD-RAE-1155-502
NEXT ASSY.	USED ON	DECIMALS ± .005, ANGLES ± 1°	CLIENT:	APPROVED			
APPLICATION				SCALE	UNIT WT		CODE SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD

NOTES: UNLESS OTHERWISE SPECIFIED:

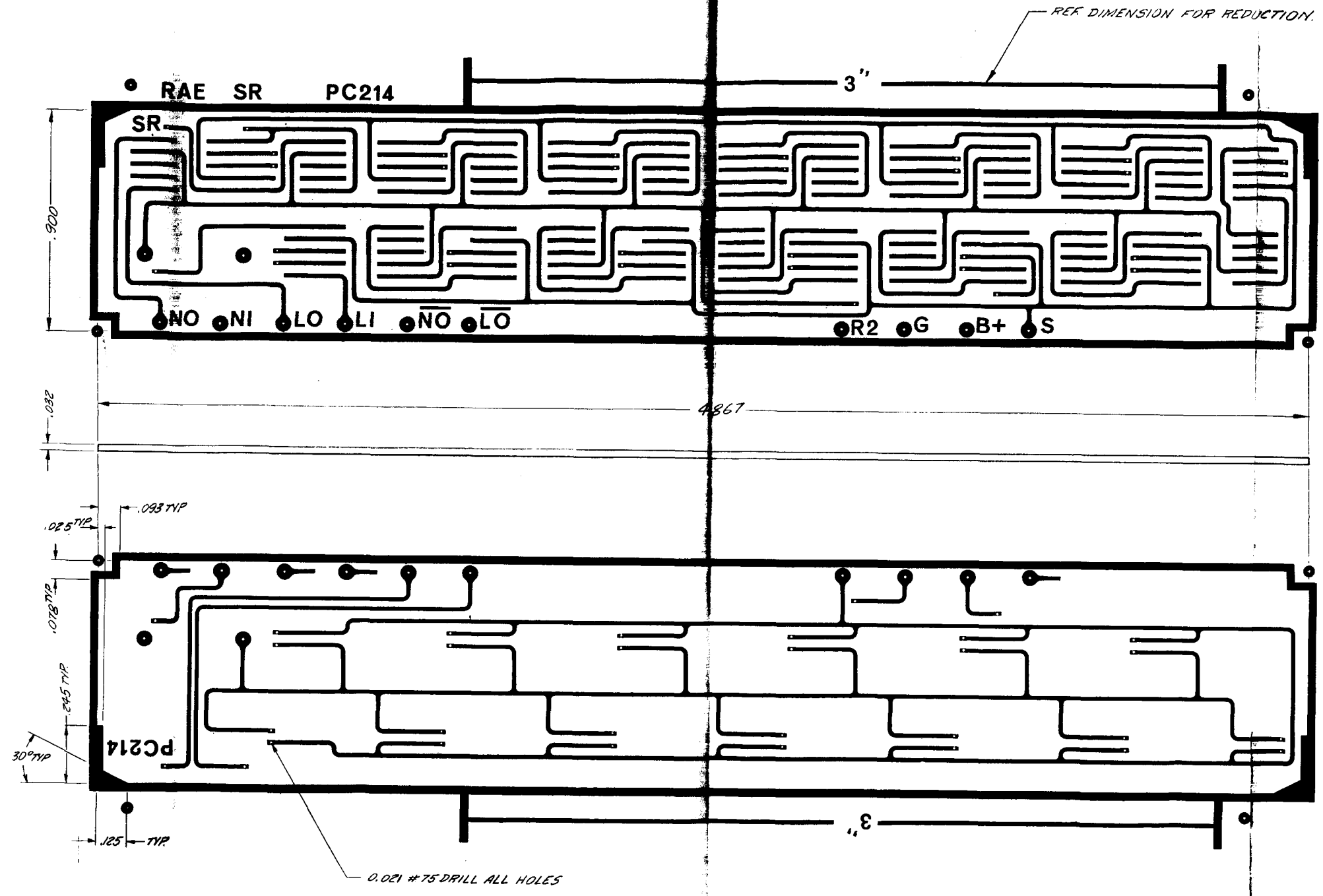
1. 63 FINISH ALL OVER
2. FILL BEND RELIEFS WITH SOLDER AFTER FABRICATION



WTA 215M-D-420

		MATERIAL 3E455	NAME	INIT	DATE	RAE	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
			DESIGNER				
			DRAWN WTA			COVER, CONTAINER	
		DO NOT SCALE THIS DRAWING	CHECKED				
		REMOVE BURRS, BREAK SHARP EDGES	APPROVED				
2331F-956		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4/1				GD-RAE-1155-500
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± 1/64	FINISH: NOTED				
APPLICATION		DECIMALS ±.005 ANGLES ± ___	CLIENT: APPROVED			SCALE / UNIT WT	CODE / SHEET OF

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE.032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154

WTA 2158-D-492

2158-D-491 NEXT ASSY.	USED ON	APPLICATION	
MATERIAL SEE NOTE 1			
DO NOT SCALE THIS DRAWING			
REMOVE BURRS, BREAK SHARP EDGES			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4/1		
TOLERANCE ON FRACTIONS ±	FINISH:		
DECIMALS ±.005, ANGLES ±1°	CLIENT:		

	NAME	INIT	DATE
DESIGNER			
DRAWN	WTA		
CHECKED			
APPROVED			
APPROVED			

RAE
PRINTED WIRING BOARD
SHIFT REGISTER

SCALE | UNIT WT

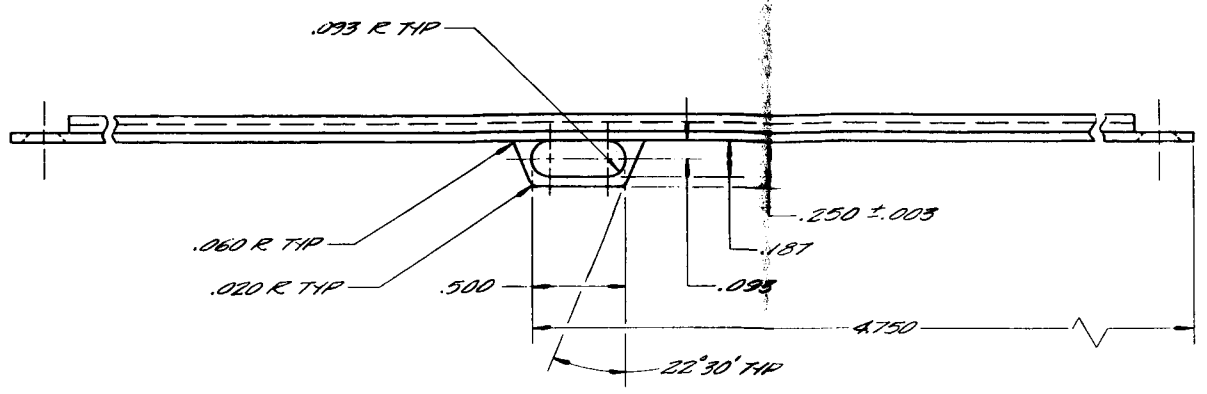
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

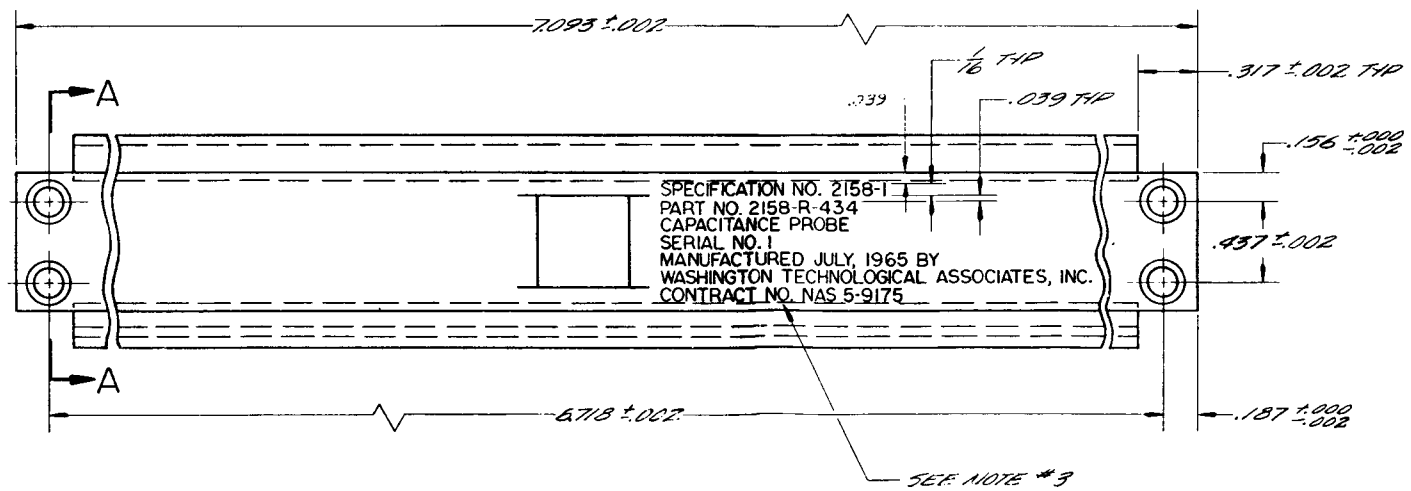
GD-RAE-1155-503

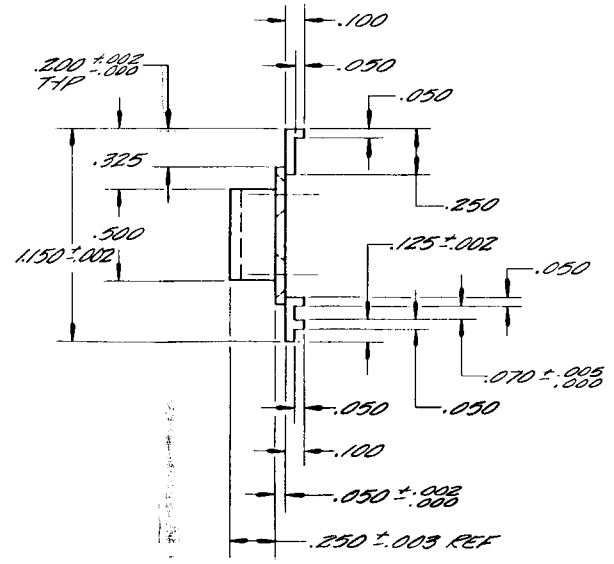
CODE | SHEET 1 OF 1

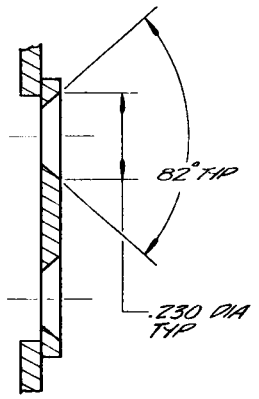
NOTES: UNLESS OTHERWISE SPECIFIED:
1. 63 FINISH ALL OVER
2. FINISH: IRIDITE #15A MIX
   ALLIED RESEARCH
   BALTIMORE, MARYLAND
3. ENGRAVE SURFACE AS SHOWN. FILL CHARACTERS WITH WHITE EPOXY ENAMEL AFTER IRIDITE FINISH.

REV	DATE	BY	DESCRIPTION	APPVD









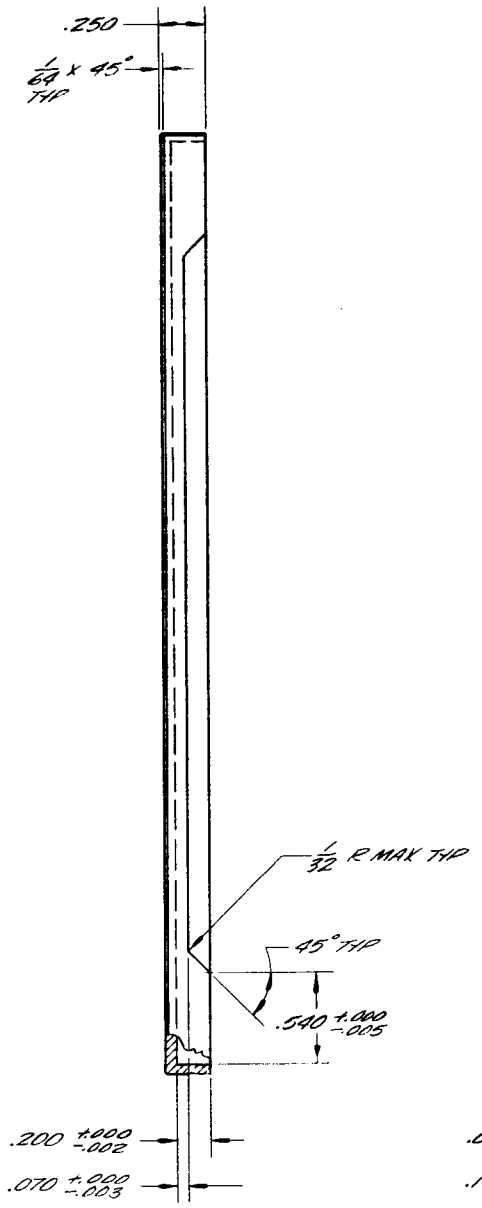
SECTION A-A
SCALE: 4/1
TYP 2 PLACES

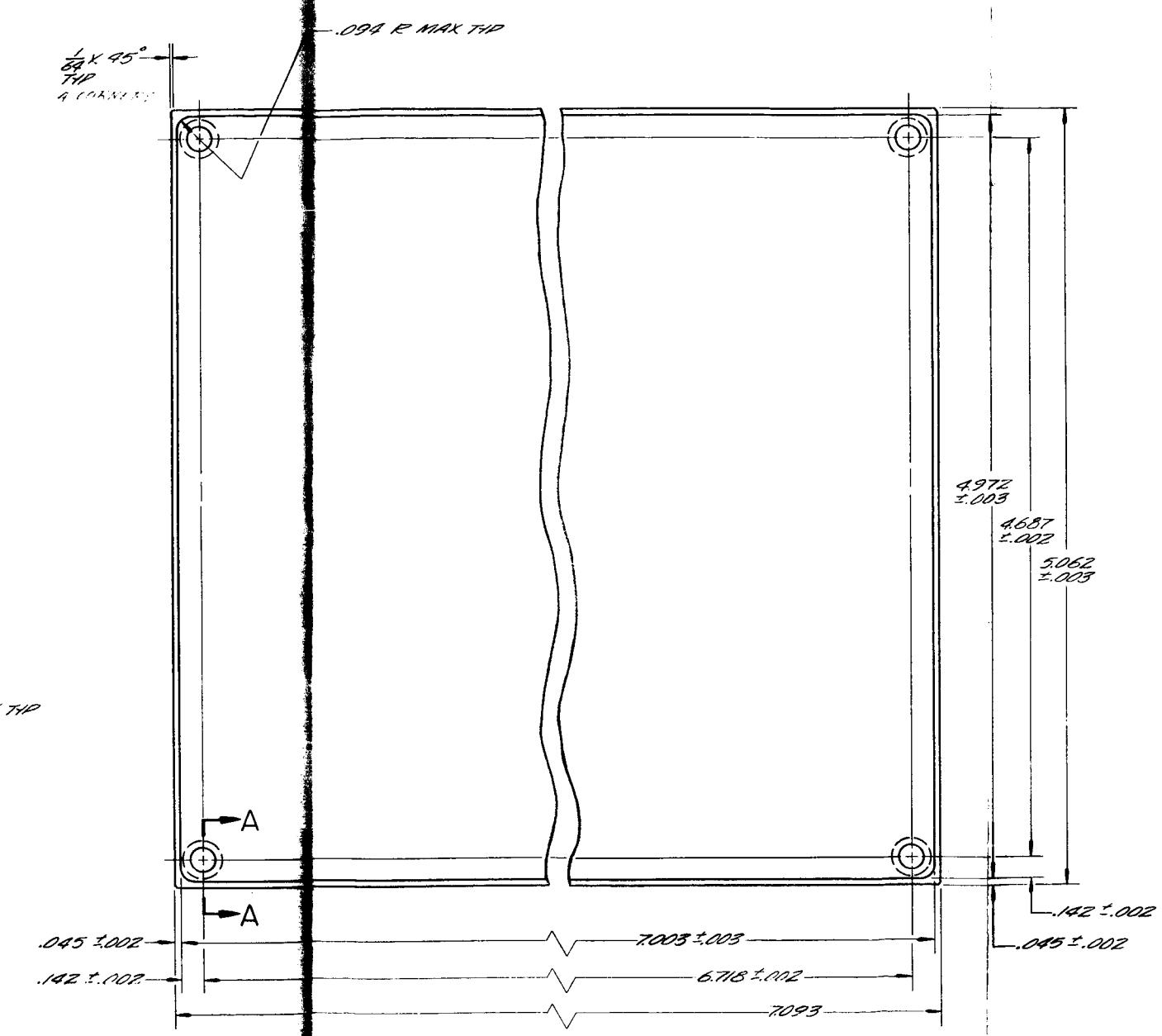
WTA 2158-D-475

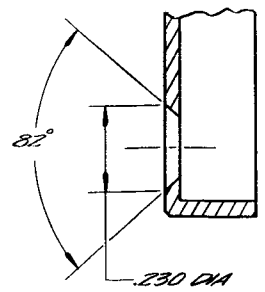
		MATERIAL MAGNESIUM AZ31B	NAME	INIT	DATE	RAE SIDE PANEL, RIGHT	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
			DESIGNER				
		DO NOT SCALE THIS DRAWING	DRAWN WTA				
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED				
2158-F-406		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON FRACTIONS ±1/64 DECIMALS ±.005, ANGLES ±2° SCALE: 2/1 FINISH: NOTE 1 CLIENT:	APPROVED				GD-RAE-1155-504
NEXT ASSY.	USED ON		APPROVED			SCALE UNIT WT	CODE SHEET 1 OF 1
APPLICATION							

NOTES: UNLESS OTHERWISE SPECIFIED:
1. 63 FINISH ALL OVER
2. FINISH: IRIDITE #15A MIL
ALLIED RESEARCH
BALTIMORE, MARYLAND

REV	DATE	BY	DESCRIPTION	APPVD







SECTION A-A
SCALE: 4/1
TYP 4 PLACES

WTA 215F-D-178

		MATERIAL MAGNESIUM AZ31B	NAME	INIT	DATE
			DESIGNER		
			DRAWN WTA		
		DO NOT SCALE THIS DRAWING	CHECKED		
		REMOVE BURRS, BREAK SHARP EDGES	APPROVED		
2153.F-D.56		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4/1 NOTED	APPROVED	
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± 1/64	FINISH: NOTED		
APPLICATION		DECIMALS ±.005; ANGLES ±	CLIENT:		

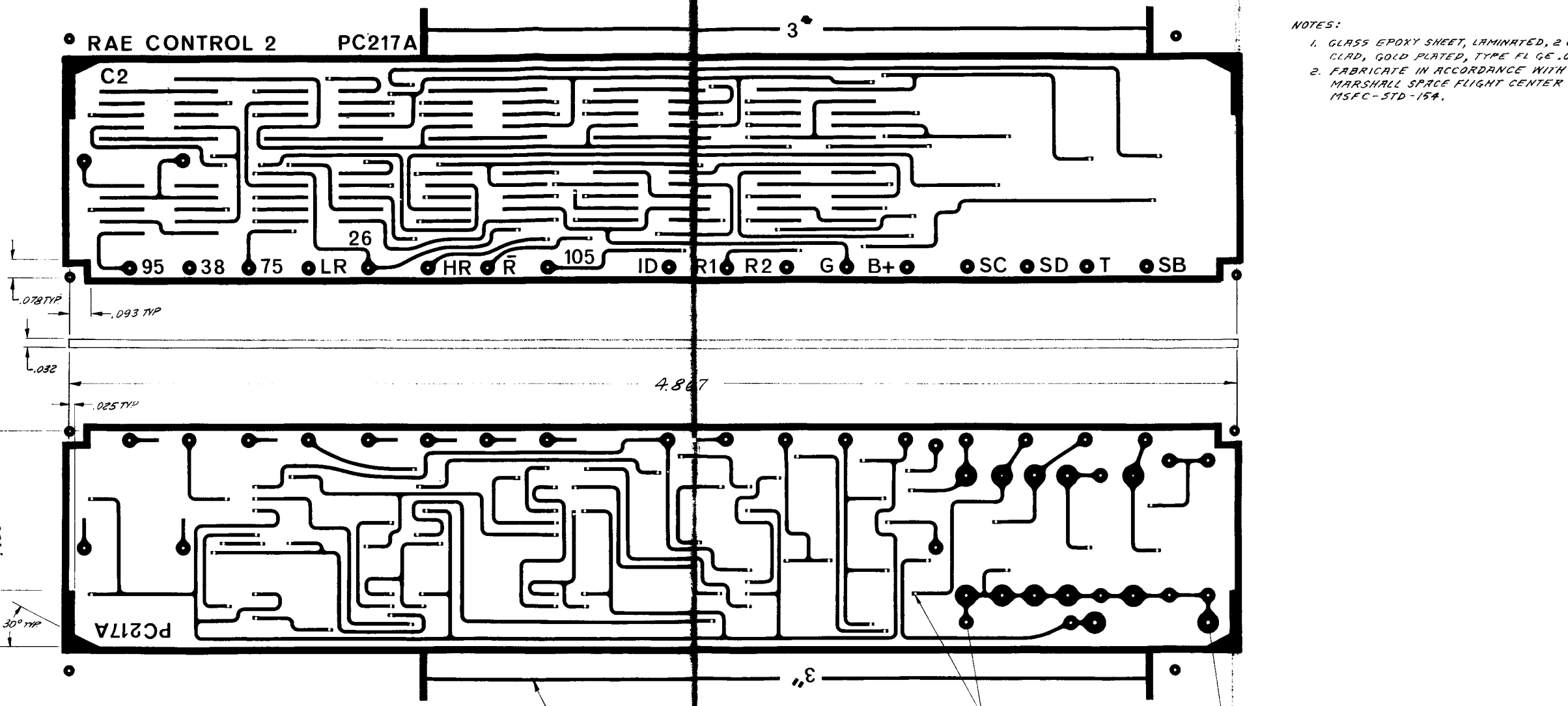
RAE
COVER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-1155-505

SCALE | UNIT WT | CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY SHEET, LAMINATED, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE .032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.

WTA 2158-D-500

2158-D-499 NEXT ASSY.	USED ON APPLICATION	MATERIAL SEE NOTE 1.	
		DO NOT SCALE THIS DRAWING	
		REMOVE BURRS, BREAK SHARP EDGES	
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1
		TOLERANCE ON FRACTIONS · DECIMALS .005 · ANGLES · 1°	FINISH:
			CLIENT:

	NAME	INIT	DATE
DESIGNER			
DRAWN	WTA		
CHECKED			
APPROVED			
APPROVED			

RAE
PRINTED WIRING
BOARD CONTROL #2

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

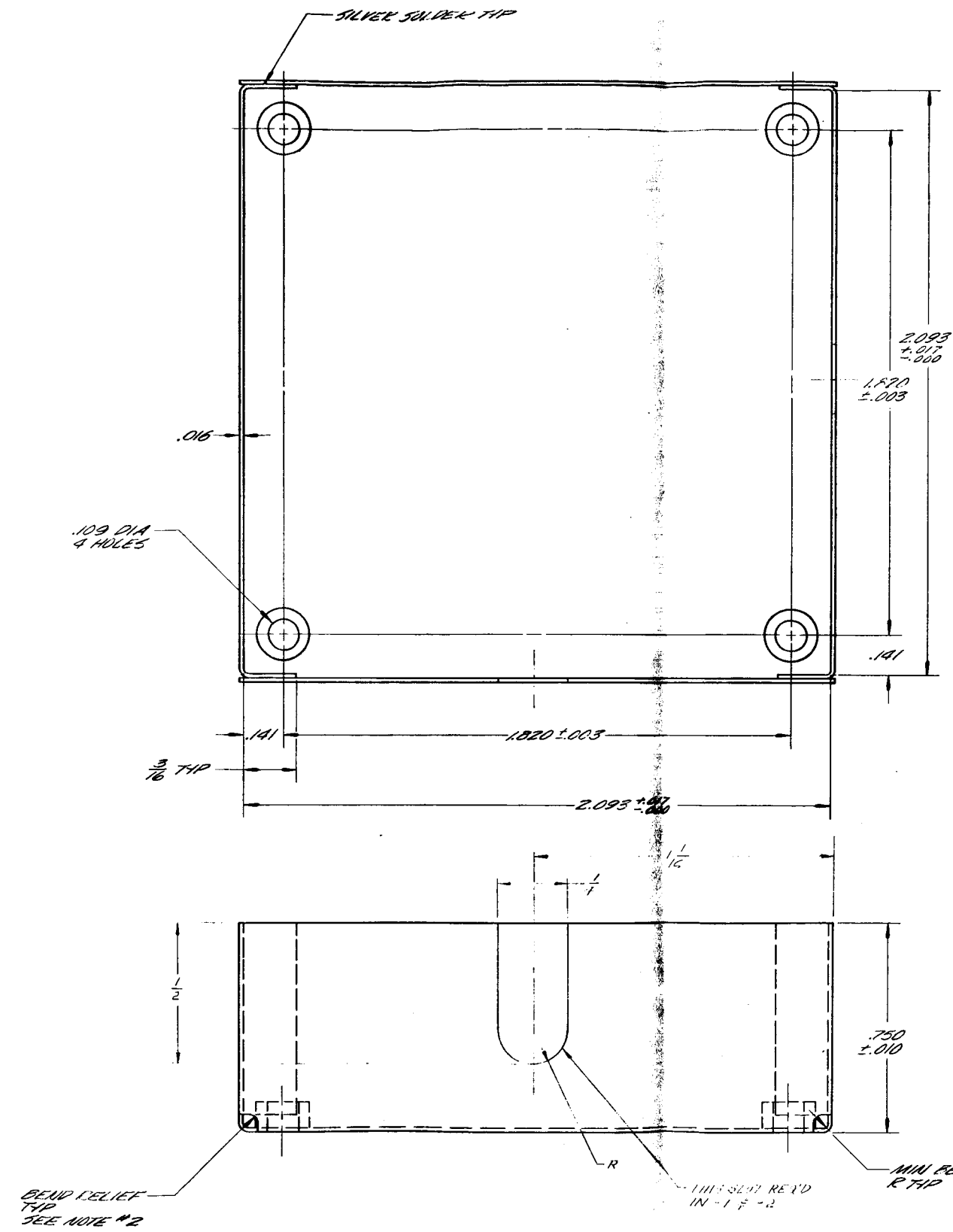
GD-RAE-1155-506

SCALE	UNIT WT	CODE	SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED:

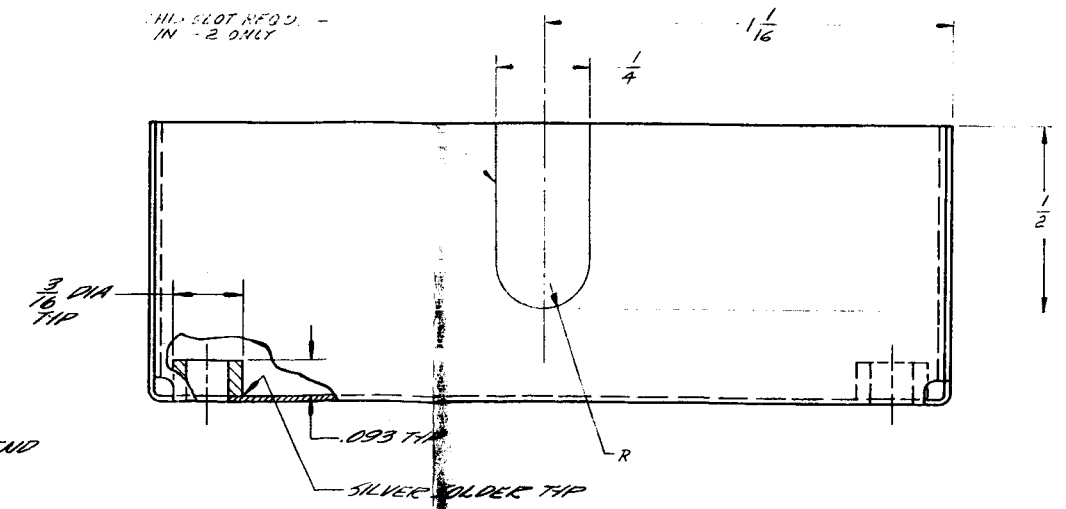
1. 63 FINISH ALL OVER
2. FILL BEND RELIEFS WITH SOLDER AFTER FABRICATION

REV	DATE	BY	DESCRIPTION	APPVD



DASH NO.	NO. OF SLOTS REQ'D.
-1	1
-2	2

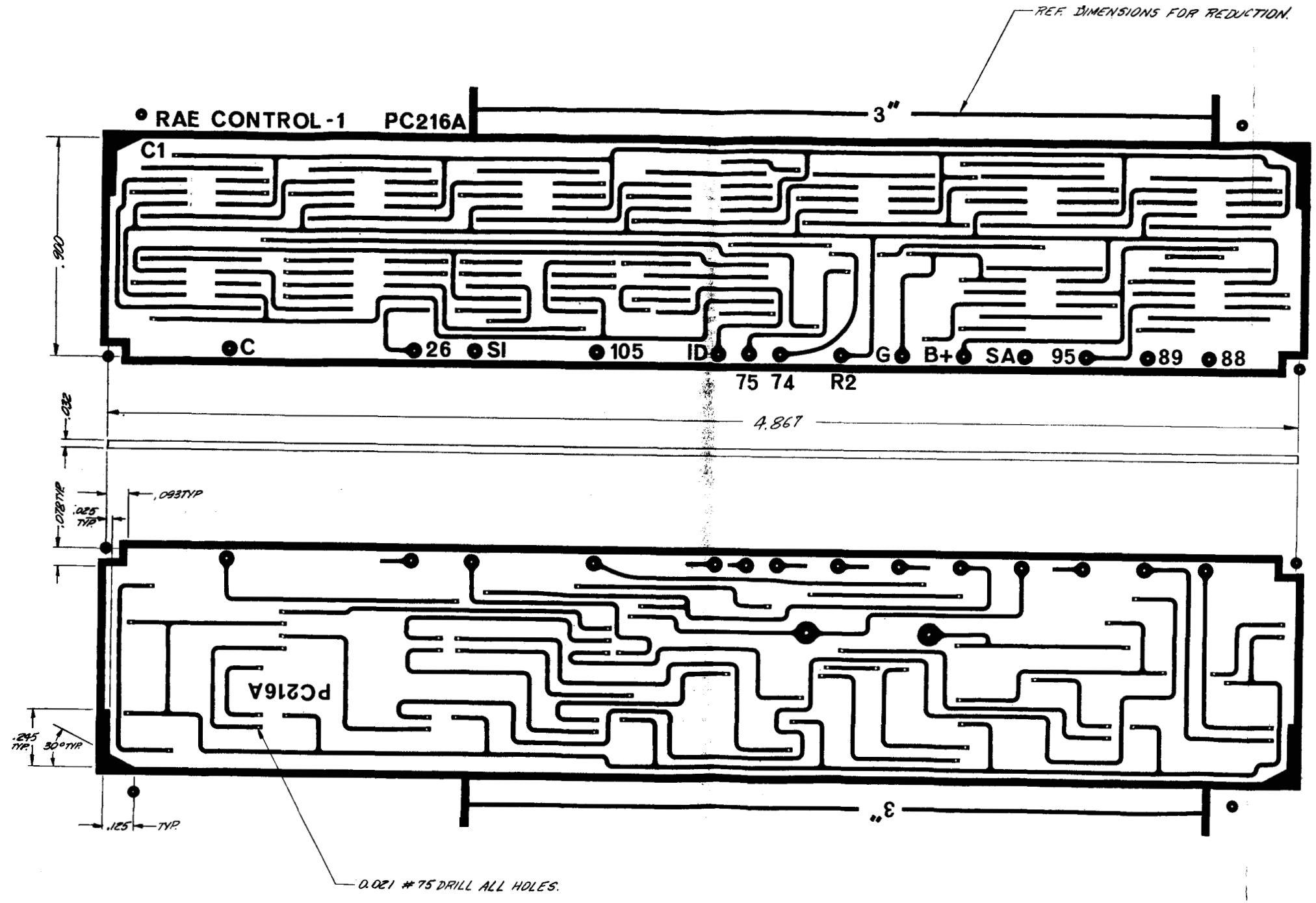
1 HOLE REQ'D. IN -2 ONLY



WTA 2158-D-479

		MATERIAL BRASS	NAME	INIT	DATE	RAE CONTAINER
		DO NOT SCALE THIS DRAWING	DESIGNER			NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
		REMOVE BURRS, BREAK SHARP EDGES	DRAWN WTA			
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED			
2158-D-406		TOLERANCE ON FRACTIONS ± 1/64	APPROVED			GD-RAE-1155-507
NEXT ASSY.	USED ON	DECIMALS ±.005. ANGLES ± —	APPROVED			
APPLICATION		SCALE: 4/1 FINISH: NOTED CLIENT:	SCALE	UNIT WT		CODE SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE .032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.

WTA 2158-D-494

2158-D-493	
NEXT ASSY.	USED ON
APPLICATION	

MATERIAL SEE NOTE 1.

DO NOT SCALE THIS DRAWING

REMOVE BURRS, BREAK SHARP EDGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON FRACTIONS ±
DECIMALS ±.005, ANGLES ±1°

SCALE: 4/1

FINISH:

CLIENT:

	NAME	INIT	DATE
DESIGNER			
DRAWN	WTA		
CHECKED			
APPROVED			
APPROVED			

RAE
PRINTED WIRING
BOARD CONTROL
CIRCUIT # 1

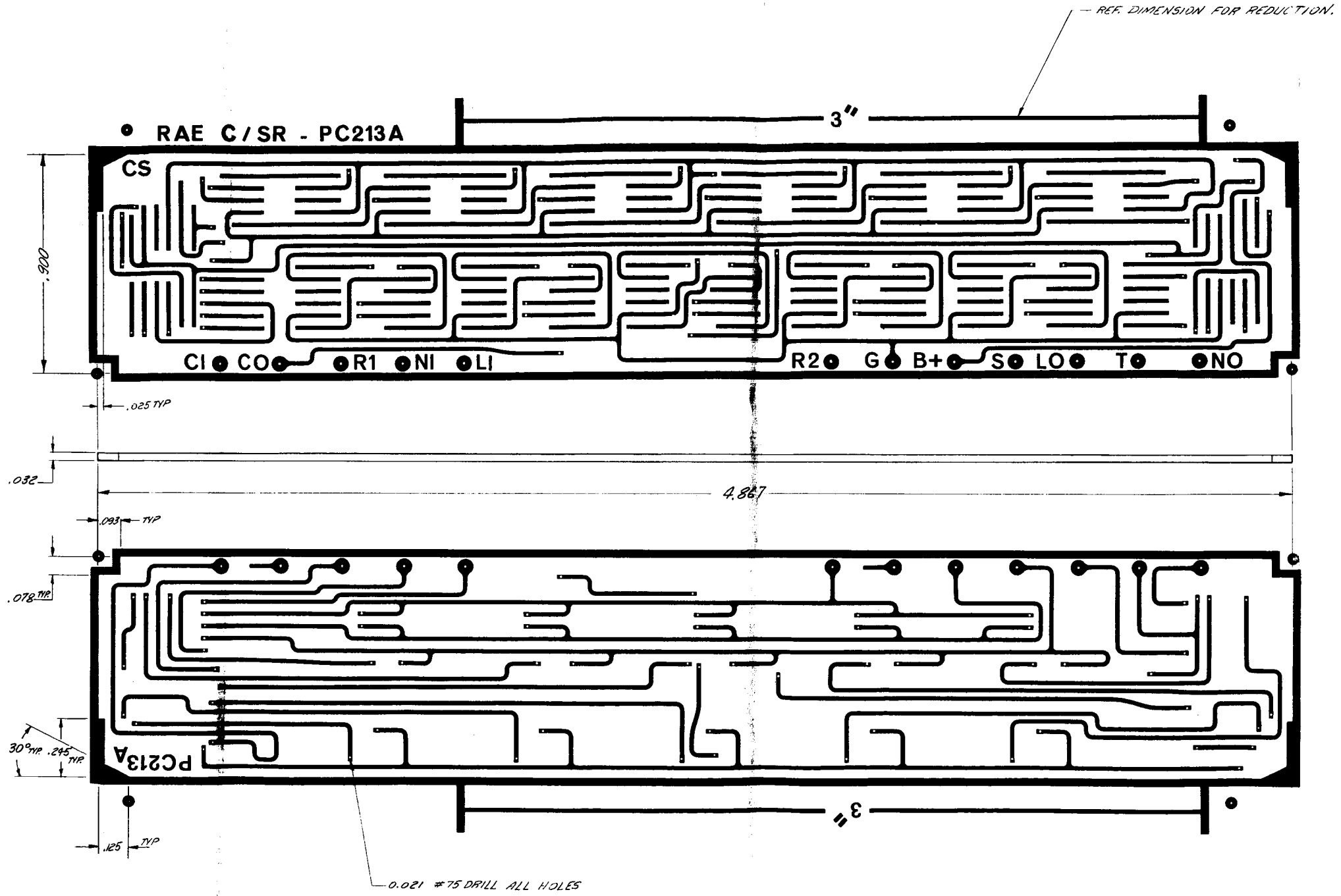
SCALE | UNIT WT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-1155-508

CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD



NOTES:

1. GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED. TYPE FL GE .032 C2.
2. FABRICATE P.C. BOARDS IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC - STD - 154.

WTA 2158-D-488

		MATERIAL SEE NOTE 1		NAME	INIT / DATE
		DO NOT SCALE THIS DRAWING		DESIGNER	
		REMOVE BURRS, BREAK SHARP EDGES		DRAWN WTA	
2158-D-487		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1	CHECKED	
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ±	FINISH:	APPROVED	
APPLICATION		DECIMALS ±.005, ANGLES ± 1°	CLIENT:	APPROVED	

RAE
PRINTED WIRING BOARD COUNTER SHIFT REGISTER

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

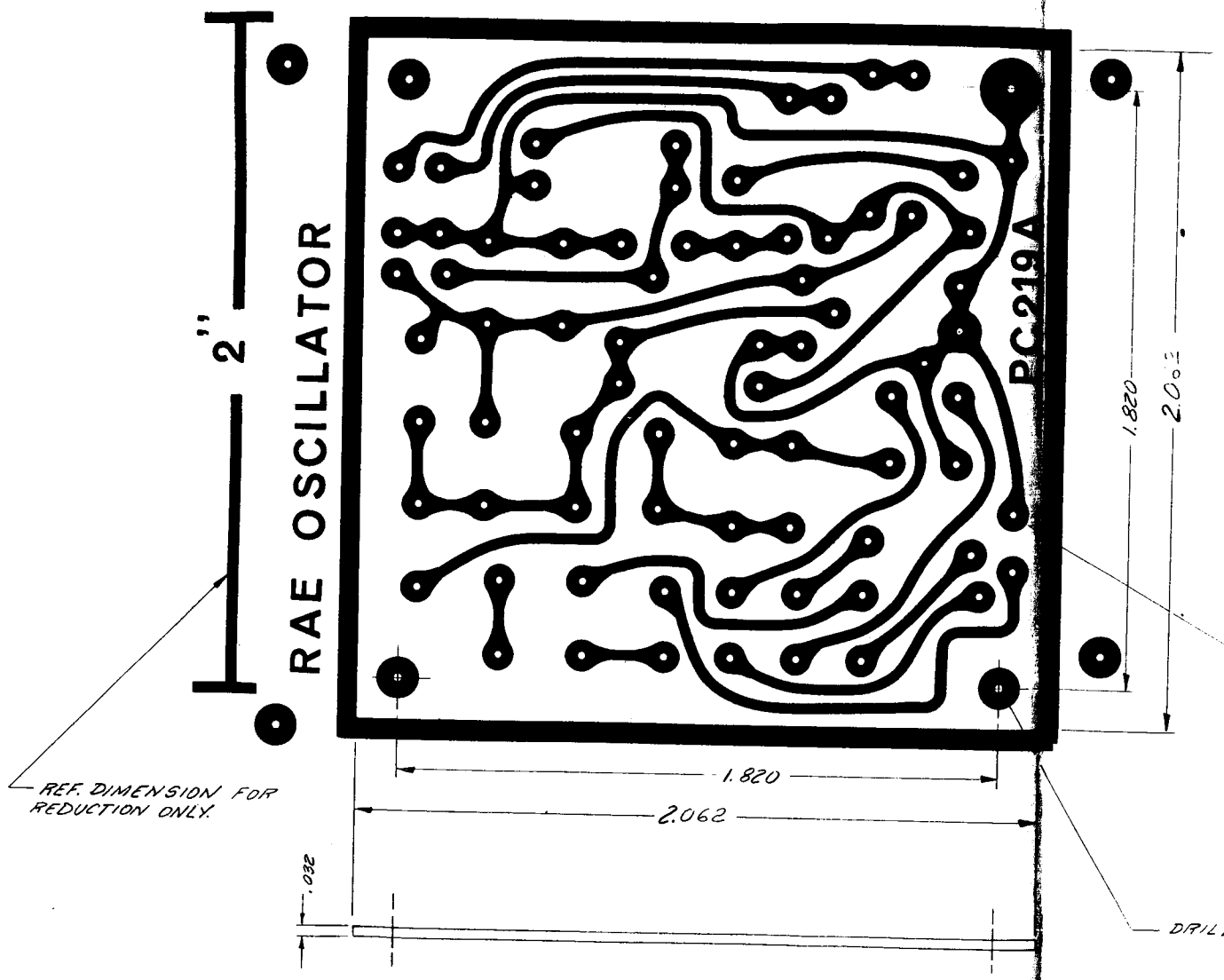
GD-RAE-1155-509

SCALE | UNIT WT | CODE | SHEET 1 OF 1

REV	DATE	BY	DESCRIPTION	APPVD

NOTES:

1. MATERIAL - GLASS EPOXY LAMINATED SHEET, 2 OZ. COPPER CLAD, GOLD PLATED, TYPE FL GE .032 C2.
2. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD MSFC-STD-154.

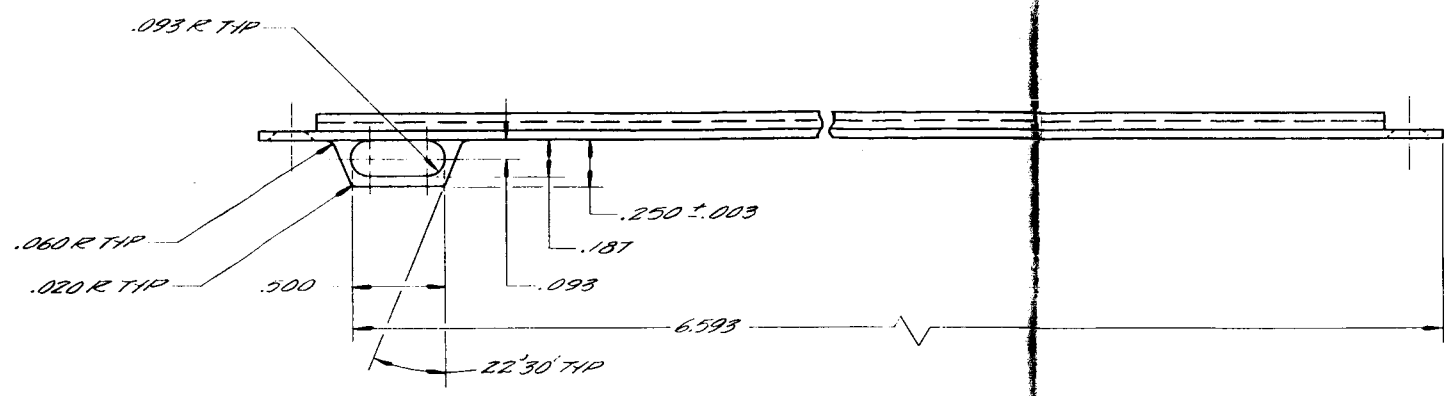


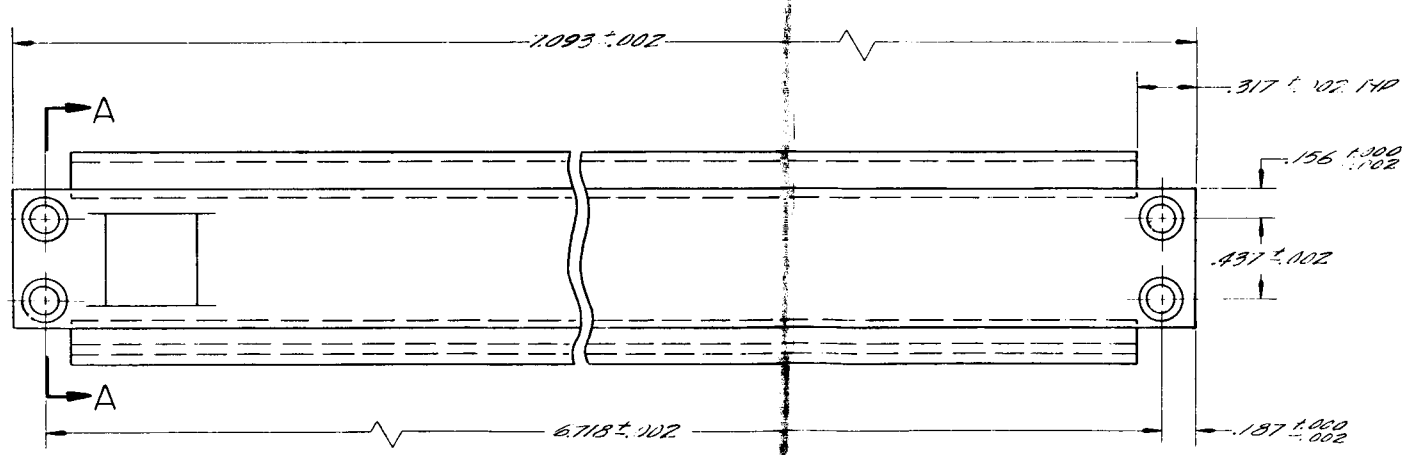
WTA 2158-D-507

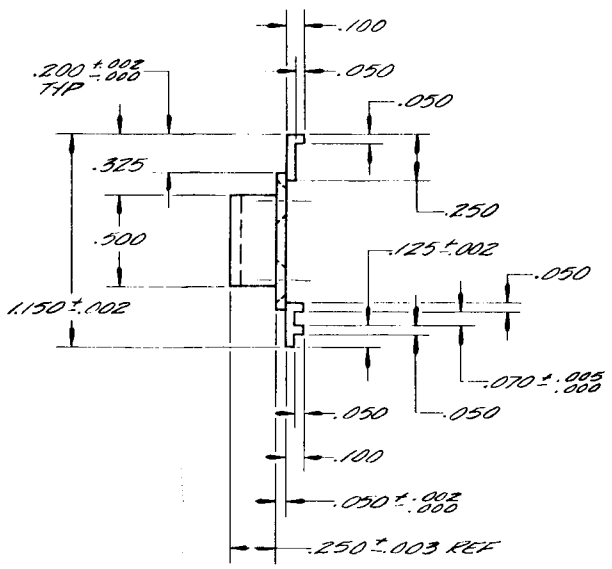
		MATERIAL SEE NOTE 1.		NAME	INIT	DATE	RAE PRINTED WIRING BOARD, RAE OSCILLAIOR	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND	
		DO NOT SCALE THIS DRAWING		DESIGNER					
		REMOVE BURRS, BREAK SHARP EDGES		DRAWN WTA					
2158-D-506 NEXT ASSY.	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 4:1	CHECKED					
APPLICATION		TOLERANCE ON FRACTIONS ± DECIMALS ± . ANGLES ±	FINISH:	APPROVED				GD-RAE-1155-510	
			CLIENT:	APPROVED			SCALE	UNIT WT	CODE SHEET 1 OF 1

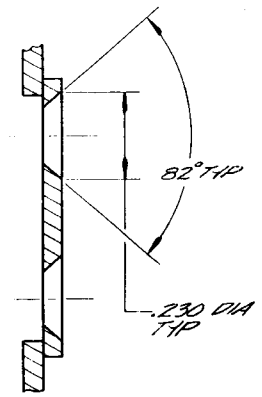
NOTES: UNLESS OTHERWISE SPECIFIED:
1. FINISH: ALL OVER
2. FINISH: IRIDITE #15A MIL
ALLIED RESEARCH
BALTIMORE, MARYLAND

REV	DATE	BY	DESCRIPTION	APPVD









SECTION A A
SCALE: 4/1
TYP 2 PLACES

WTA 2158-D-474

		MATERIAL MAGNESIUM AZ31B	NAME	INIT	DATE
			DESIGNER		
		DO NOT SCALE THIS DRAWING	DRAWN WTA		
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED		
2153-F-436		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: 3/4 1/2	APPROVED	
NEXT ASSY.	USED ON	TOLERANCE ON FRACTIONS ± 1/64	FINISH: IRIDITE	APPROVED	
APPLICATION		DECIMALS ± .005 ANGLES ± 2°	CLIENT:		

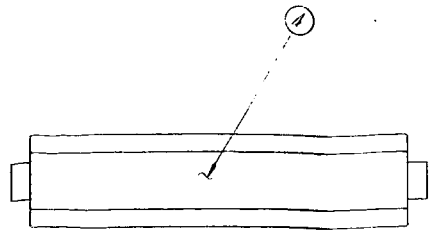
RAE
SIDE PANEL, LEFT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD-RAE-1155-511

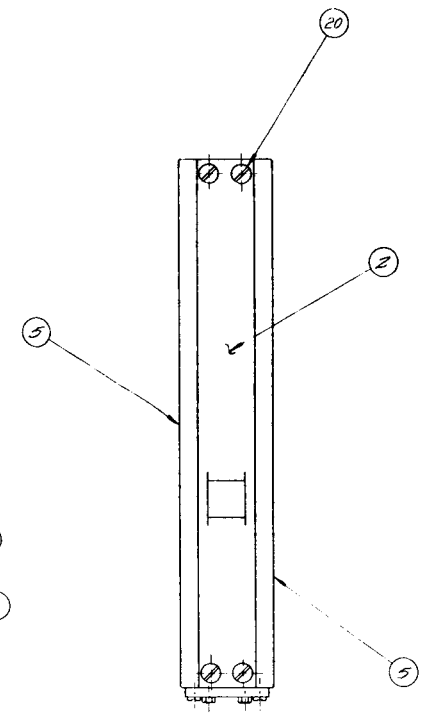
SCALE | UNIT WT | CODE | SHEET 1 OF 1

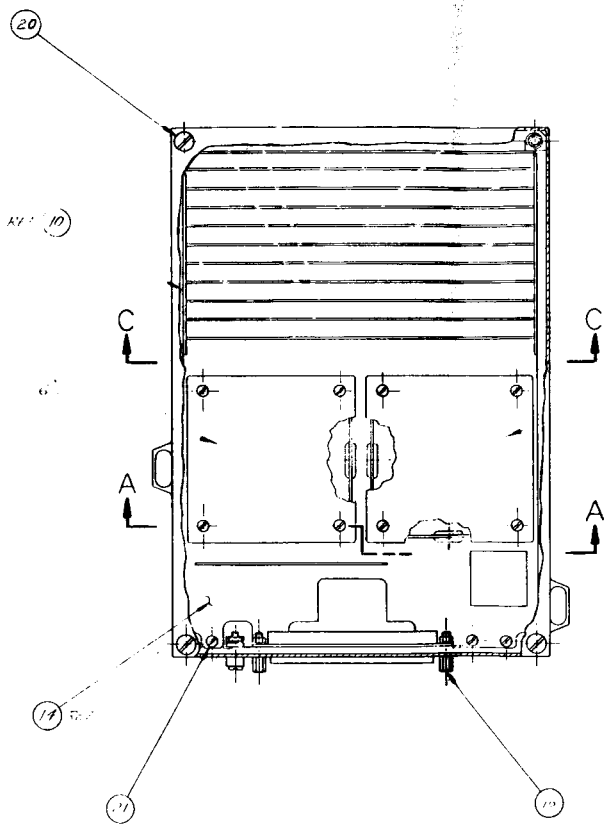
REV	DATE	BY	DESCRIPTION	APPVD

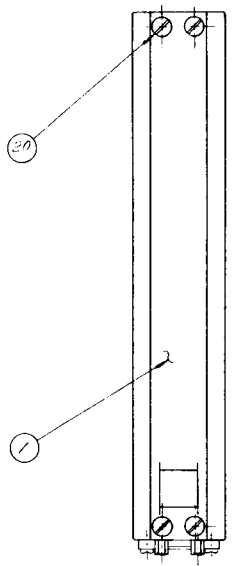


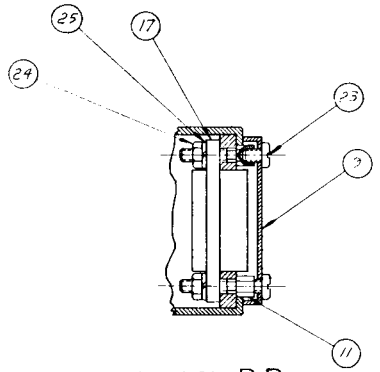
NOTES:

1. SOLDER PER NASA QUALITY PUBLICATION NPC 200-4



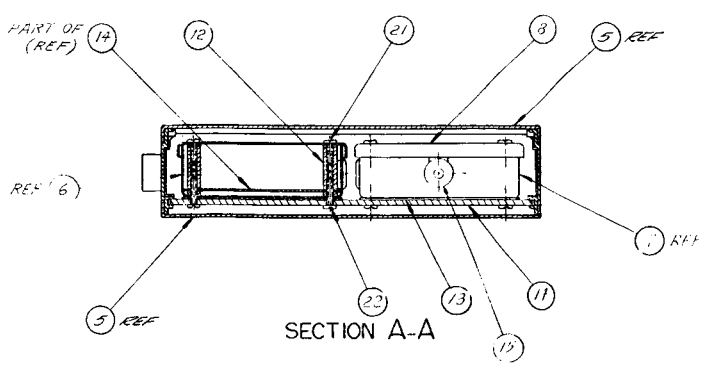




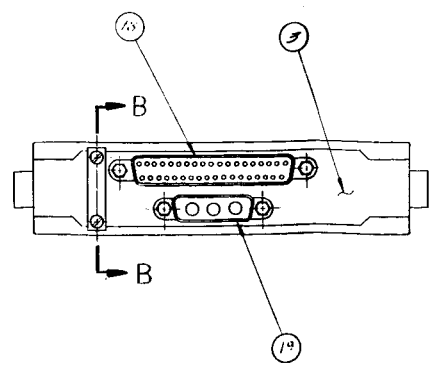


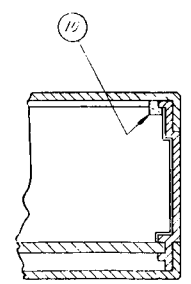
SECTION B-B

SCALE: 2/1



SECTION A-A





SECTION C-C

SCALE: 2/1

ITEM NO.	NO. REQ'D	NOMENCLATURE	DWG. NO. or DESIG. OF MFG'S PART NO.	MATERIAL	REMARKS	ZONE
25	2	WASHER, LOCK, SPLIT		18/8 CRES OR 300 SERIES	#2 NOM. I.D. ALLMETAL SCREW PROD. GARDEN CITY, N.Y.	
24	2	NUT, HEX, SMALL PATTERN			#2-56 UNC-2B	
23	2	SCREW, MACH, PAN HD, SMALL PATTERN			#2-56 UNC-2B × 1/8 LG	
22	8	SCREW, MACH, PAN HD, SMALL PATTERN			#2-56 UNC-2B × 3/8 LG	
21	11	SCREW, MACH, PAN HD, SMALL PATTERN			#2-56 UNC-2B × 1/4 LG	
20	16	SCREW, MACH, 82° FLAT HD.		18/8 CRES OR 300 SERIES	#4-40 UNC-2A × 5/16 ALLMETAL SCREW PROD. GARDEN CITY, NY	
19	1	CONNECTOR	DAM-3W3P-NMC-2		CANNON ELECTRIC CO., LOS ANGELES, CAL.	
18	1	CONNECTOR	DCM-37P-NMC-2			
17	1	SOCKET	MDB1-215-N001			
16	4	SCREW LOCK ASS'Y	D-20418-2	NON-MAGNETIC	CANNON ELECTRIC CO, LOS ANGELES, CALIF.	
15	3	GROMMET	MS 35489-1	RUBBER		
14	1	PRINTED WIRING, ASS'Y, MAIN	2158-R-501			
13	2	BOARD, INSULATOR	2158-B-485			
12	8	SPACER	2158-B-484			
11	2	STANDOFF	2158-B-483			
10	2	RETAINING STRIP	2158-C-482			
9	1	CAN	2158-B-481			
8	2	COVER, CONTAINER	2158-D-480			
7	1	CONTAINER	2158-D-479-2			
6	1	CONTAINER	2158-D-479-1			
5	2	COVER	2158-D-478			
4	1	PANEL, REAR	2158-C-477			
3	1	PANEL, FRONT	2158-F-476			
2	1	SIDE PANEL, RIGHT	2158-D-475			
1	1	SIDE PANEL, LEFT	2158-D-474			

LIST OF MATERIAL FOR ONE SURVEY ITEM

IN 2154 F 480

MATERIAL	NAME	INIT	DATE
DO NOT SCALE THIS DRAWING	DESIGNER		
REMOVE BURRS, BREAK SHARP EDGES	DRAWN WTA		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED		
TOLERANCE ON FRACTIONS ± ___ DECIMALS ± ___ , ANGLES ± ___	ISSUED: 7/8/65	APPROVED	
NEXT ASSY. USED ON APPLICATION	FINISH: CLIENT:	APPROVED	

RAE
CAPACITANCE PROBE ELECTRONICS ENCLOSURE ASSEMBLY

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

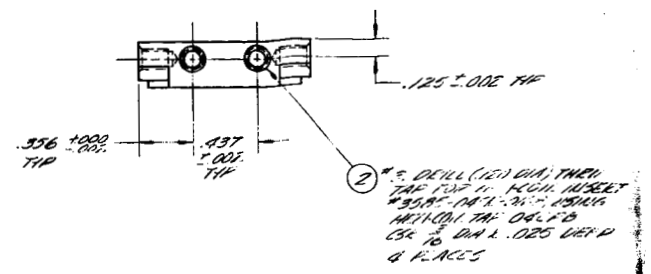
GF-RAE-1155-512

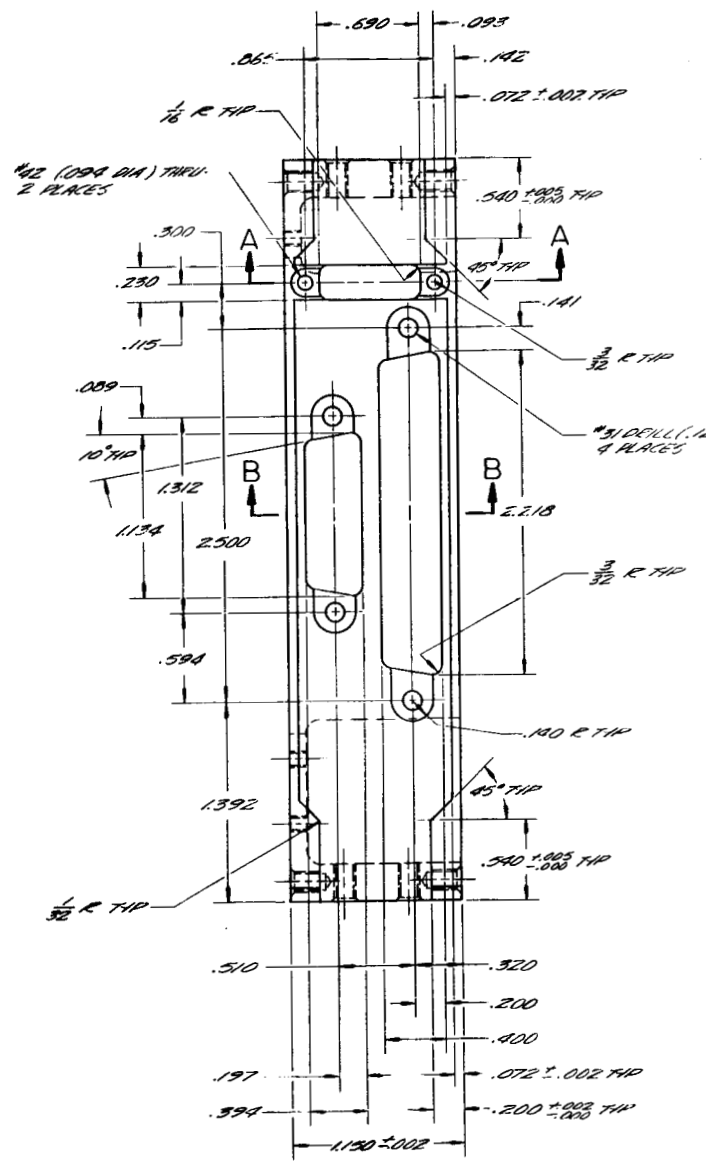
SCALE | UNIT WT | CODE | SHEET 1 OF 1

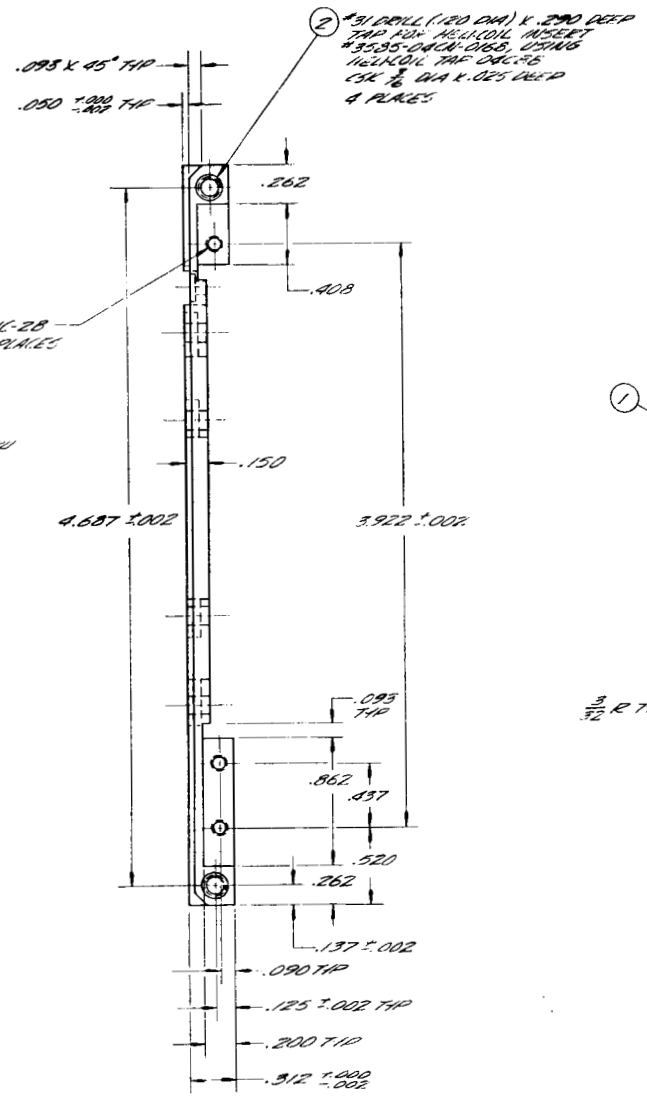
SYM	DATE	BY	DESCRIPTION	APPVD

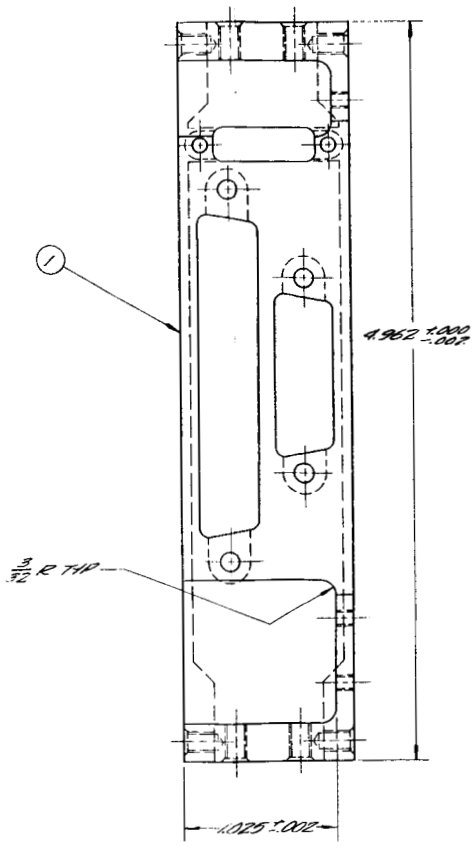
NOTES: UNLESS OTHERWISE SPECIFIED:

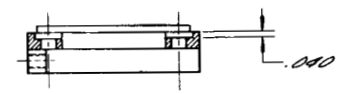
1. 63 FINISH ALL OVER
2. FINISH: IRIDITE # 15 A MIL ALLIED RESEARCH BALTIMORE, MARYLAND
3. INSTALL HELICOIL INSERTS WET WITH ZINC CHROMATE PRIMER AFTER FINAL FINISH



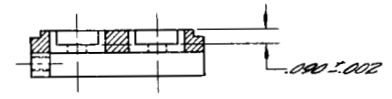








SECTION A-A



SECTION B-B

WTA 2158-F-476

ITEM NO.	QTY REQD	NOMENCLATURE	MATERIAL	REMARKS
2	B	HELI-COIL	#3539-DACR-DRD	AERO-MAGNETIC HELICOIL CORPORATION DANBURY, CONN.
1	—	FRONT PANEL	AL. ALLOY STOCK, AE 31B	5" X 1 3/8" X 3/8" THK

LIST OF MATERIAL

WTA-2158 F-476

		MATERIAL SEE LIST OF MATERIAL	NAME	INIT	DATE
			DESIGNER		
		DO NOT SCALE THIS DRAWING	DRAWN WTA		
		REMOVE BURRS, BREAK SHARP EDGES	CHECKED		
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SCALE: FULL	APPROVED	
		TOLERANCES ON FRACTIONS ± 1/64	FINISH: AS IS		
NEXT ASSY.	USED ON	DECIMALS ± .01'S. ANGLES ± 1°	CLIENT:	APPROVED	
	APPLICATION				

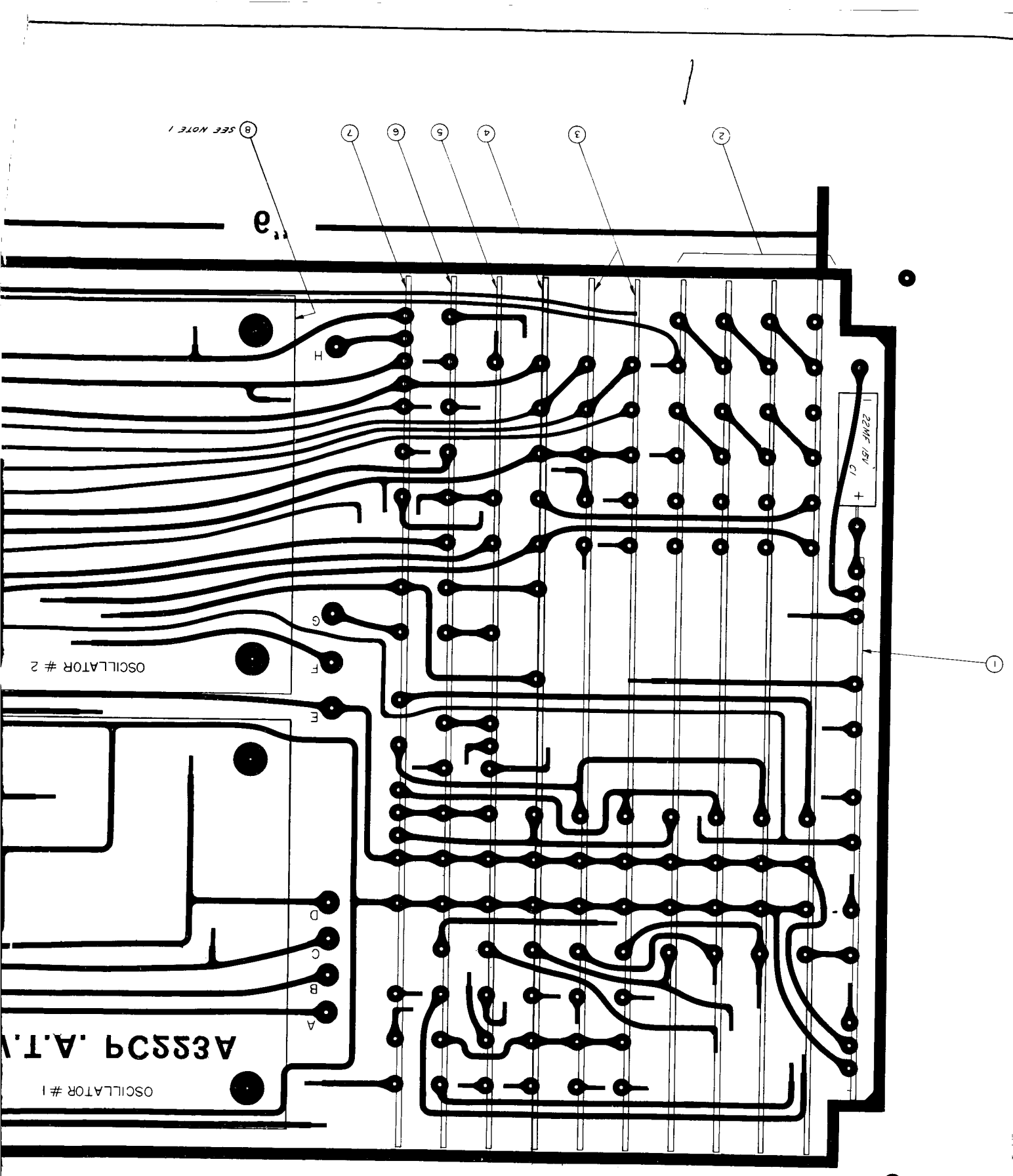
RAE

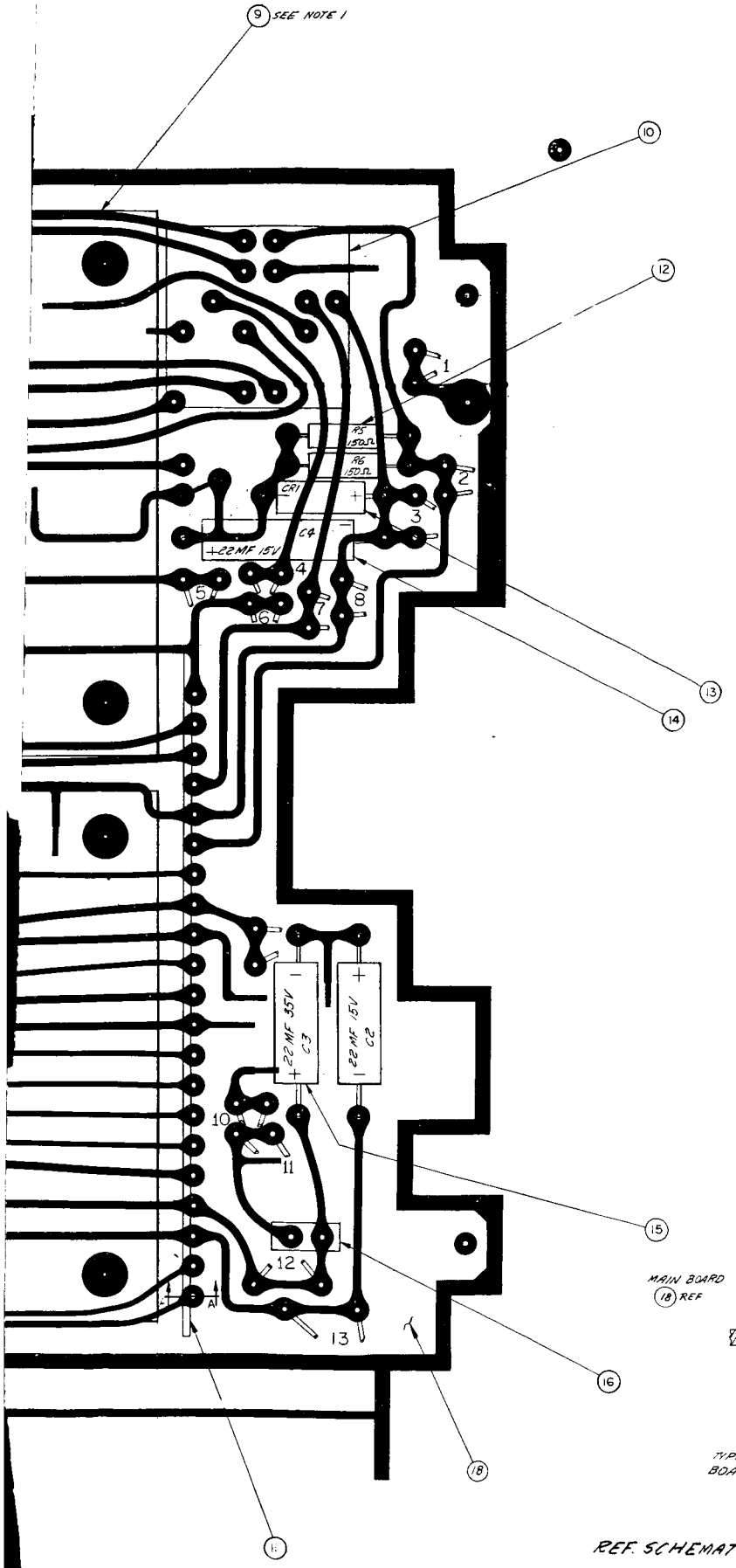
PANEL, FRONT

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GF-RAE-1155-513

SCALE | UNIT WT | CODE | SHEET 1 OF 1


SEE NOTE 1
8
7
6
5
4
3
2
1
H
G
F
E
D
C
B
A
OSCILLATOR # 2
OSCILLATOR # 1
22MF 16V

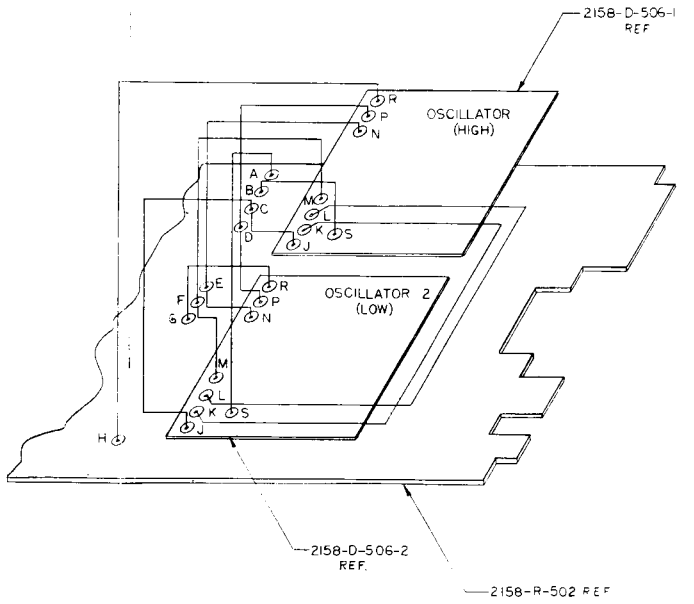


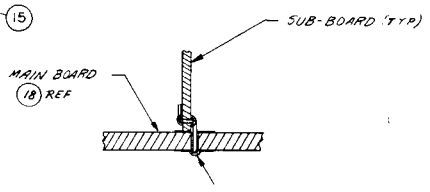
(17)

LIST OF OUTPUT WIRES				
FROM POINT	WIRE DESCRIPTION	COLOR	APPROX LENGHT	TO CONNECTOR PIN
1	CHASSIS GND	BRN	3"	J2 9-10
2	+15 VOLT	WHT/BLU	3"	J2 17-18
3	POWER GND	BLK	3"	J2 11-12
4	400 CPS CLOCK	WHT/ORN	3"	J2 23-24
5	+3.5 VOLTS	ORN	3"	J2 13-14
6	READ COMMAND	WHT/GRN	3"	J2 21-22
7	DATA OUT	WHT/YEL	3"	J2 25-26
8	SIGNAL GND	GRY	3"	J2 15-16
9	SHIFT COMMAND	WHT/BRN	3"	J2 19-20
10	SHIELD GND	WHT	3"	J2 7-8
11	TEMP MONITOR	VIO	3"	J2 3-4
12	+12 VOLTS	RED	3"	J2 1-2
13	-6 VOLTS	BLU	3"	J2 5-6

NOTES:

1. LEAVE 8" MIN. LENGTH EXTENDING FROM OSCILLATOR TERMINALS TO INSURE SUFFICIENT WIRE FOR USE TO PASS WIRES THRU GROMMETS PRESSED INTO SLOTS IN CANS (2158-D-473) I.C. TERMINALS INDICATED ON OSCILLATORS, ITEMS 8 & 9, SHOULD BE MOUNTED INTO RESPECTIVE CANS AS SHOWN. SEE DRAW NG 2158-F-486 FOR MECHANICAL ASSEMBLY
2. SOLDER PER NASA QUALITY PUBLICATION NPC-250-1
3. FABRICATE IN ACCORDANCE WITH GEORGE C. MARSHALL SPACE FLIGHT CENTER STANDARD PROCEDURE NO. [illegible]





SECTION A-A

TYPICAL INSTALLATION OF SUB-BOARDS TO MAIN BOARD.

REF. SCHEMATIC 2158-R-529

2

ITEM NO.	NO. REQD	NOMENCLATURE	DWG NO. & DESIGNATION OR MFGS PART NO.	MATERIAL	REMARKS	ZONE
18	1	PRINTED WIRING BOARD, MAIN	2158-C-502			
17	4R	WIRE, TEFLON CORTED	# 26 AWG	STRANDED	FOR INDIVIDUAL COLORS SEE TABLE	
16	1	TEMP MONITOR			SUPPLIED BY [illegible]	
15	1	CAPACITOR, 22 MFD 35V.	SPRAGUE			
14	3	CAPACITOR, 22 MFD 15V	SPRAGUE			
13	1	DIODE IN749A	T.I.			
12	2	RESISTOR 150Ω 1/4W ±5%	WELWYN			
11	1	P.C. TEST LIMITER	2158-D-495			
10	1	WELDED MODULE	2158-D-527			
9	1	OSCILLATOR (HIGH)	2158-D-506-1			
8	1	OSCILLATOR (LOW)	2158-D-506-2			
7	1	P.C. ASSY. CONTROL #3	2158-D-504			
6	1	P.C. ASSY. CONTROL #2	2158-D-499			
5	1	P.C. ASSY CONTROL #1	2158-D-493			
4	1	P.C. ASSY. H.C. COUNTER S/P	2158-D-489			
3	2	P.C. ASSY. COUNTER SHIFT R.	2158-D-487			
2	4	P.C. ASSY. SHIFT REG.	2158-D-491			
1	1	P.C. ASSY. CONTROL #4	2158-C-497			

LIST OF MATERIAL FOR ONE SUBJECT ITEM WTA 2158-R-5

DRAWING NO'S INVOLVED:	NAME	INIT	DATE
NEXT ASSY: 2158-F-486	DESIGNER		
DO NOT SCALE THIS DRAWING	DRAWN WTA		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED		
SCALE: 4:1	APPROVED		
TOLERANCES: FRACTIONS ± ANGLES ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ±	JOB NO:		
	CLIENT:		
	APPROVED		

RAE
PRINTED WIRING ASSY
MAIN

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT MARYLAND

GR-RAE 1155-514

SCALE | UNIT WT | CODE | SHEET 1 OF 1